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A 100nm Copper/Low-K Bulk CMOS Technology with Multi Vt and Multi Gate Oxide Integrated Transistors for Low Standby Power, High Performance and RF/Analog System on Chip Applications

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Abstract: We report a 100nm modular bulk CMOS technology platform with multi Vt and multi gate oxide integrated transistors that enables device and circuit co-design [1] techniques (e.g., well biasing and power down/reduction) for low standby power (LSP), high performance (HP), high speed (HS), and RF/Analog system on chip (SoC) applications. The transistor performances are comparable or better than recently reported data at the 100nm technology node (see Table 1). This technology also features an all-layer copper/low-k (<3.0) interlayer dielectric (ILD) backend for speed improvement and dynamic power reduction [2].

Process Integration & Device Design Features: Table 1 concisely shows the specifications of the low standby power (LSP), high performance (HP), high speed (HS), I/O and analog devices supported for system on chip (SoC) applications. Three I/O options for 3.3V, 2.5V and 1.8V Vdd applications are supported by 70Å, 50Å and 35Å Tox transistors, respectively. Dual Vt options are offered in each device type. These multi-Vt and multi gate oxide integrated transistors have various performance levels and off-state leakage differentiation from tens of pA/μm to tens of nA/μm.

This modular CMOS technology platform offers the flexibility of combining transistors of varied performance levels, off-state leakage and Vdd to best meet diverse SoC product requirements. An example SoC process sequence is shown in Fig. 1 to integrate the 65nm Lpoly/18Å Tox HP transistors and 80nm Lpoly/24Å Tox LSP transistors with 50Å I/O devices. The triple gate oxide (TGO) integration and transistor optimization are employed to ensure that the same SPICE model and library file are applicable for each transistor type in both the usual dual gate oxide (DGO) and TGO integration. Fig. 2 shows a vertically straight poly gate profile for the 45nm sub-nominal high speed (HS) transistors (nominal Lpoly is 50nm). Also included in Fig. 2 is a XTEM of the ~15Å oxynitride gate oxide underneath the poly gate. Fig. 3a shows that transistors in this 100nm technology node are successful in delivering the necessary device performance improvement for the LSP, HP and HS devices based on historical trends from 130nm [8] and 180nm [6,7] technology nodes.

Device and Circuit Co-design for LSP, HP and HS SoC: As technology scales down to 100nm node and beyond, a new paradigm of device and circuit co-design [1] is required to meet the competing requirements of high performance and low standby/dynamic power. For instance, Fig. 3b shows that LSP-Hvt devices may support die cost reduction and ~15% performance improvement due to device scaling for a high volume consumer wireless product migrating from 130nm to 100nm technology node. However, further performance improvement with the same standby power requires LSP-Lvt devices with higher drive currents while relying on well bias to minimize standby power. HP devices are required to meet the minimum performance requirement for the third generation (3G) data-rich wireless SoC applications. Due to lower body factor, well biasing on these low Vt and high Ioff transistors only offer <2x Ioff reduction. Thus, low leakage LSP transistors in the TGO process is needed as cut-off devices to implement power down/reduction circuit techniques to minimize standby power for 3G wireless applications.

Multi Gate Oxide Integration and Optimization for Performance, Standby and Dynamic Power: Out of the three multi gate oxide integration methods investigated, brute-force TGO (BF-TGO) with optimized strip/pre-clean offers no mobility degradation, resistance to boron penetration and flexibility in integrating gate oxides of >5Å thickness difference. Contrary to what was reported in [4], F19 causes excessive PMOS Vt shift/scatter due to boron penetration. SIMS data also show boron penetration through the gate oxide. N14 implant method is only able to reduce oxynitride Tox by <5Å (Fig. 4). Optimization of S/D ext. module and halo profile by multi halo implants results in manufacturing-friendly transistors (Fig. 6-7) with comparable or better Ion/Ioff and AC performances than recently reported data (Table 1 and Fig. 5). SRAM Icc is minimized with optimized narrow width PMOS made possible by an optimized STI module and an anneal [7] (Fig. 9a). Fig. 8 shows that minimal silicon recess due to optimized process flow leads to reduction of S/D ext. resistance and thus improvement, especially, in linear drive current. Transistor structures are optimized to suppress the impact of merged spacers due to narrow poly-to-poly spacing w/o sacrificing short channel margin (Fig. 9b). Dynamic power reduction and speed improvement are achieved through the use of all-layer dual in-laid Cu metalization and low-k (<3.0) ILD.

RF/Analog Device Features: Low voltage (1.5-1.8V) analog transistors with low Vt and low output conductance are formed by S/D extension engineering without using additional masks [9]. We have also developed high voltage (2.5V or 3.3V) low Vt transistors for high performance analog design. A full suite of high quality passives including MIM capacitors, thin film metal resistors and inductors is integrated into the technology and fully characterized.

Reliability & Manufacturing Assessment: Reliability of the 18Å gate oxide in BF-TGO with optimized strip/pre-clean is shown to be similar to DGO control in Fig. 10(a). Fig. 10(b) shows that the 100nm technology node high density 1.33μm^2 SRAM bitcell yields about 35μA cell current and has 240mV of static noise margin (SNM). Both the 80nm/24Å LSP and 65nm/18Å HP transistors were built with BF-TGO using a 130nm node mask set and demonstrated better or comparable 4Mb SRAM yield as compared to the DGO control (Fig. 10).

Conclusions: We have developed a 100nm copper/low-k modular bulk CMOS technology platform with multi Vt and multi gate oxide integrated transistors that can be combined with well biasing and power down/reduction techniques to meet the requirements of LSP, HP and RF/Analog system on chip applications.

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References

[1] M. Fukuma et al., VLSI Tech., 2000.
[2] S. Parihar et al., IEDM, 2001.
[3] K. Miyashita et al., VLSI Tech., 2001, and A. Oishi et al, IEDM, 2001.
[4] Y. Goto et al., VLSI Tech., 2000, and A Ono et al., IEDM, 2001.
[5] S.-F. Huang et al., IEDM, 2001.
[6] P. Gilbert et al., IEDM, 1998.
[7] G. C-F Yeap et al., VLSI Tech., 2000.
[8] A. Perera et al., IEDM, 2000.
[9] A. Chatterjee et al., IEDM, 2001.

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Table 1 Low Standby Power (LSP), High Performance (HP), High Speed (HS), I/O and Analog device comparison with recently reported data

Transistor	Low Standby Power (LSP)				High Performance (HP)					High Speed (HS)				I/O		Analog	
	High Vt	Ref. [3]	Low Vt	Ref. [3]	Low Vt	Ref. [3]	Ref. [5]	High Vt	Ref. [3]	Low Vt	Ref. [5]	Ref. [3]	High Vt	50Å	70Å	High Perf.	Low Volt.
V_{DD} (V)	1.2	1.2	1.2	1.2	1.2(1.0)	1.2(1.0)	1.2(1.0)	1.2(1.0)	1.2(1.0)	1.0	1.0	1.0	1.0	3.3	2.5	2.5	1.5
Lpoly (nm)	80	85	80	85	65	70	-	65	65	50	50	60	50	380	280	280	250
Tox (nm)	2.4	2.4	2.4	2.4	1.85	1.9	1.6	1.85	1.9	1.55	1.4	1.6	1.55	7.0	5.0	5.0	2.4
I_{on} (μA/μm)	420/180	380/155	575/245	575/240	910/410 (690/290)	845/385 (-/-)	-/- (700/295)	735/325 (530/230)	730/325 (-/-)	905/405	870/370	815/370	780/335	575/ 280	580/ 280	670/ 335	550/ 250
I_{off} (nA/μm)	0.02	0.02	0.6	0.6	20	10	20	2	2	100	100	30	10	0.003	0.003	0.5	0.1
Jg (A/cm²)	0.002	0.001	0.002	0.001	0.5	0.1	-	0.5	0.1	20	-	10	20	-	-	-	-
Cov(fF/μm)	0.28/0.25	-	0.28/0.25	-	0.31/0.28	-	-	0.31/0.28	-	0.31/0.28	-	-	0.31/0.28	-	-	-	-
Cj (fF/μm²)	0.8	-	0.8	-	0.8	-	-	0.8	-	0.8	-	-	0.8	0.8	0.8	0.8	0.8
I_{off} reduction by Well Bias	~10x	-	~10x	-	###	-	-	~5x	-	###	-	-	~ <5x	-	-	-	-

<2x Ioff reduction by well bias. Need voltage modulation (power down/reduction) to minimize standby power.

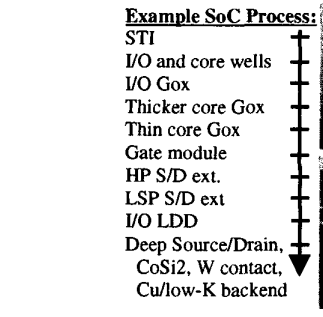

Fig.1 HP, LSP and I/O devices integrated in triple gate oxides.

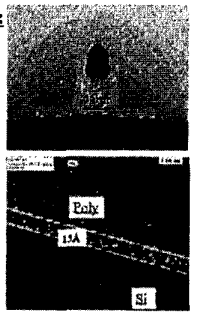

Fig.2 XTEM of 45nm sub-nominal HS transistor and ~1.5nm Tox.

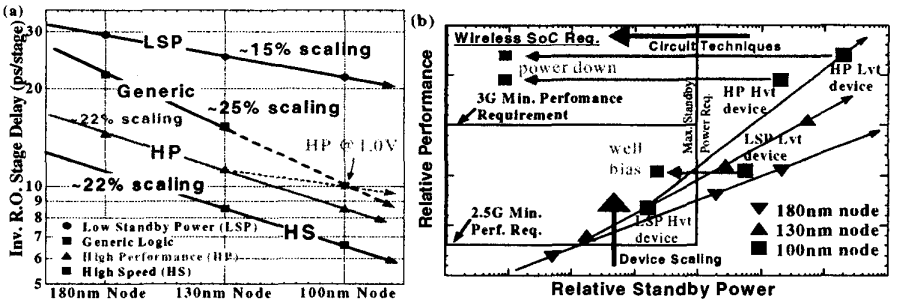

Fig.3 (a) 100nm node delivers the device performance improvement trends from 130nm [8] and 180nm [6,7] nodes. (b) Device scaling and well bias scheme enable LSP Hvt and Lvt transistors to meet 2.5G wireless SoC requirements. Device-circuit co-design: 3G wireless data rich SoC requirement met by power down technique enabled by HP/LSP transistors in the triple gate oxide SoC flow

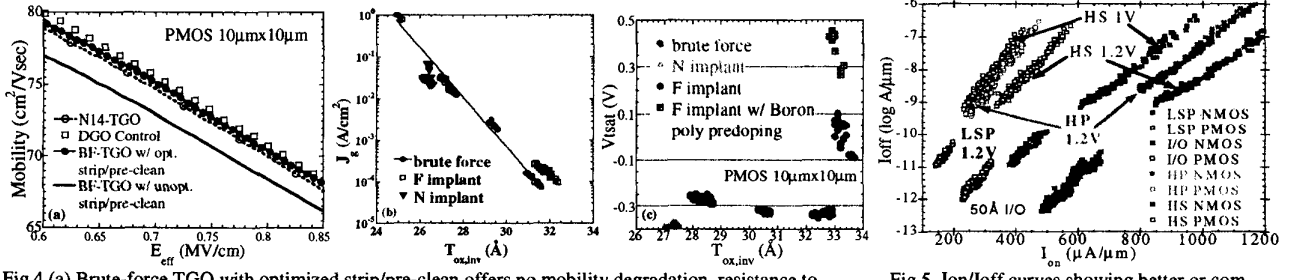

Fig.4 (a) Brute-force TGO with optimized strip/pre-clean offers no mobility degradation, resistance to boron penetration and flexibility in integrating gate oxides of >5Å thickness difference. (b) N14 TGO method is only able to reduce Tox by <5Å. (c) F19 implant causes excessive boron penetration.

Fig.5 Ion/Ioff curves showing better or comparable performances than recently reported transistors data at the 100nm tech. node [3-5].

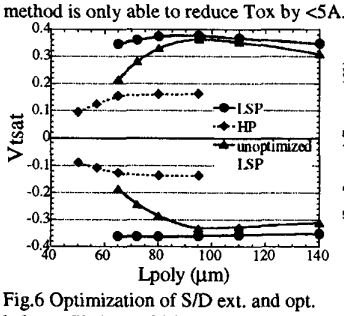

Fig.6 Optimization of S/D ext. and opt. halo profile by multi-halo implants achieves superior Vtsat roll-off characteristics.

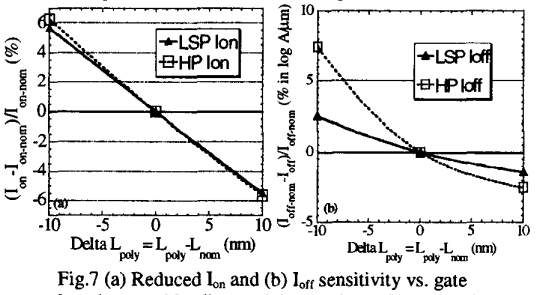

Fig.7 (a) Reduced I_{on} and (b) I_{off} sensitivity vs. gate length control leading to tight transistor characteristics for robust manufacturability.

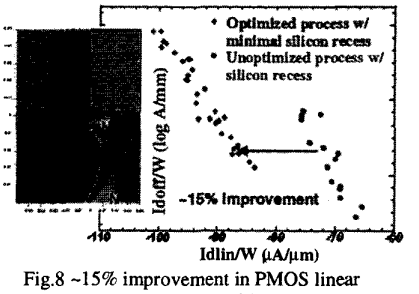

Fig.8 ~15% improvement in PMOS linear drain current due to lower S/D extension resistance by reducing Si recess

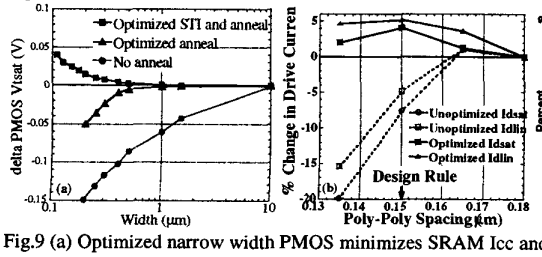

Fig.9 (a) Optimized narrow width PMOS minimizes SRAM Icc and standby power w/o impacting Icell. (b) Devices optimized to <5% Id variation suppressing poly spacing impact w/o sacrificing Vt roll-off.

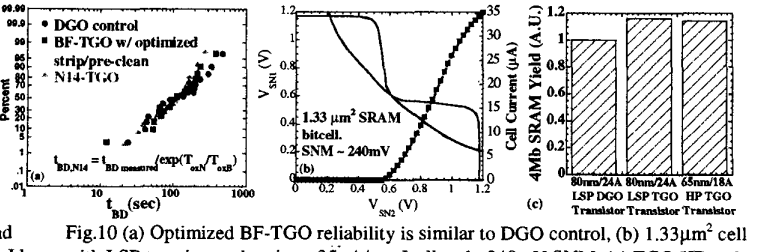

Fig.10 (a) Optimized BF-TGO reliability is similar to DGO control, (b) 1.33μm² cell with LSP transistors showing ~35μA/μm Icell and ~240mV SNM. (c) TGO HP and LSP transistors showing better or comparable 4Mb SRAM yield with DGO control.