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A 180nm Copper/Low-k CMOS Technology with Dual Gate Oxide Optimized for Low Power and Low Cost Consumer Wireless Applications

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Abstract: We report a 180nm CMOS technology with dual gate oxide (DGO) optimized for low power and low cost consumer wireless products. To minimize cost and maximize manufacturability, super halo is used for the first time to integrate 70Å 2.5-3.3V I/O devices with either 130nm/29Å or 150nm/35Å low leakage (LL) pA/μm devices, eliminating three normally-required masks. Core LL devices optimized for 1.5V and 1.8V are available to maximize circuit design compatibility and IP reuse. Both LL devices yield superior performance, and less I_{on}/I_{off} sensitivity vs. gate-length control for robust manufacturing as compared to recently reported LL devices (see Table. 1). This technology also features an all-layer copper/low-k interlayer dielectric (ILD) backend for speed improvement and dynamic power reduction [1].

Key Wireless Baseband Technology Requirements: Consumer wireless products such as cell phones pose unique technology requirements not suitably addressed by high-performance microprocessor CMOS technology [1-3]. Specific technology issues that require attention are: (1) low cost (mask count, process simplification and reuse) yet with robust manufacturing margin for high yield, (2) minimization of standby and dynamic power, (3) V_{DD} options on core devices to accommodate legacy and advanced designs for maximum IP reuse, and (4) 2.5-3.3V DGO for flexible I/O. A low power/cost 180nm wireless Cu/low-k CMOS technology has been developed to address these issues.

Process Integration & Device Design Features: Super halo [4] is utilized for the first time to integrate pA/μm LL devices with 70Å DGO without two additional channel Vt adjust masks. The high Vt needed for LL devices is achieved through channel doping increase by self-aligned tilt halo implants after gate formation. This super halo process provides the benefits of both channel and drain engineering while saving a total of three masks as compared to the conventional channel Vt approach (Fig. 1). X-SEM pictures of the core LL devices are shown in Fig.2. Only the super halo approach allows independent device optimization: retrograded well implants to optimize 70Å device Vt, and pocket implants with energy, dose, tilt and twist angle optimization for 29Å or 35Å LL devices while sharing the same well. This fact is evident in Fig. 3 showing an excessively high 70Å device Vt if additional masks are not employed in the channel Vt approach.

Super halo devices demonstrate much better short channel margin as seen in the flatter Vt roll-off (Fig. 3). The devices exhibit about 10% more drive than channel Vt devices if I_{off} is matched at the sub-nominal L_{gate}. Ideally, the L_{min} device should be targeted at the peak of the Vt_{sat} hump to meet the max. I_{off} requirement, and maximize the nominal L_{gate} drive. Fig. 4 highlights the superiority of super halo in minimizing I_{off} and I_{on} sensitivities vs. L_{gate} control, resulting in a tighter distribution of device characteristics for robust manufacturing and high yield. Super halo devices also exhibit 3-5% lower junction and Miller capacitance, and 18% less body effects.

Optimization for Standby and Dynamic Power: I_{off} sensitivity is further reduced by optimizing resist thickness and super halo implants with respective to design rules to avoid shadowing effects (Fig.5). An optimal anneal is inserted before transistors are formed to reduce diode leakage (Fig. 6) and minimum width PMOS I_{off}. The ΔVt (from 10μm to minimum width of 0.22μm) improves by 40% from 136mV to 80mV. SRAM I_{CC} leakage thus decreases from 2.3pA/bit to 1pA/bit. S/D extensions are optimized to avoid GIDL/BTBT limiting of the pA/μm device I_{off} (Fig. 7). All these optimization leads to minimization of standby power. Dynamic power reduction and speed improvement are achieved through the use of all-layer dual in-laid Cu metalization and low-k (3.5 vs. 4.1 TEOS) ILD.

Multi-Voltage Core and I/O Compatibility: Table. 1 shows the super halo LL devices have better performance than other recently reported LL devices. The availability of 150nm/35Å and 130nm/29Å LL devices present V_{DD} options of 1.8V or 1.5V to accommodate legacy and advanced designs for maximum IP reuse. The I_{on} vs. I_{off} curves for various devices are shown in Fig. 8. The migration form 150nm/35Å to 130nm/29Å allows either approximately 20% speed gain at 1.8V or 45% reduction in dynamic power at 1.5V (Fig. 9).

Reliability & Manufacturing Assessment: Fig. 10a shows both types of devices exhibit comparable DC lifetime (within device/wafer/lot variations). Super halo devices show tighter and better breakdown voltages (Fig. 10b) due to less boron/phosphorus out-diffusion to oxide for super halo implants applied after gate oxide and poly reox. Butterfly curves of a 6T SRAM cell show functionality down to 0.5V (Fig. 11). Both super halo 130nm/29Å and 150nm/35Å devices produce comparable or better megabit SRAM yield than the conventional channel Vt devices (Fig. 12).

Conclusions: We have developed a low power/cost, manufacturable, and robust 180nm copper/low-k CMOS technology that has been optimized to meet the key requirements for current and future low cost consumer wireless applications.

References

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Table. 1 Comparison of Low Leakage Device Performance

	This Work	Ref. [5]	This Work	Ref. [6,7]
V_{DD}	1.5V or *(1.8V)*	1.5V	1.8V	1.8V
L_{gate}	130nm	130nm	150nm	160nm
$T_{phys.\ ox}$	29Å	26Å	35Å	32Å
I_{on}(μA/μm)	455/175 *(650/240)*	450/170	571/205	500/180
I_{off} (pA/μm)	1/1	1/1	1/1	1/1
C_i (fF/μm^2)	1.22/1.41	1.6/1.05	1.45/1.48	1.2/1.2

 0-7803-6305-4/00/$10.00 © 2000 IEEE

Acknowledgements: The authors wish to thank APRDL process engineering, pilot line, physical analysis lab, and the management support from Bob Yeargain and Fabio Pintchovski.

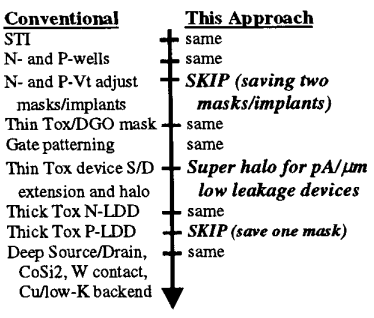

Fig.1 The super halo approach saves two well masks and a P-LDD mask in 29Å/70Å or 35Å/70Å DGO integration, and enables robust I_{off} and I_{on} control.

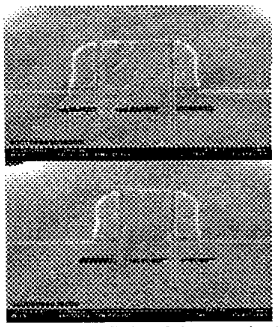

Fig.2 X-SEMs of the nominal 150nm/35Å device (L_{min}=125nm) and the 105nm L_{min} device (nominal device is 130nm/29Å).

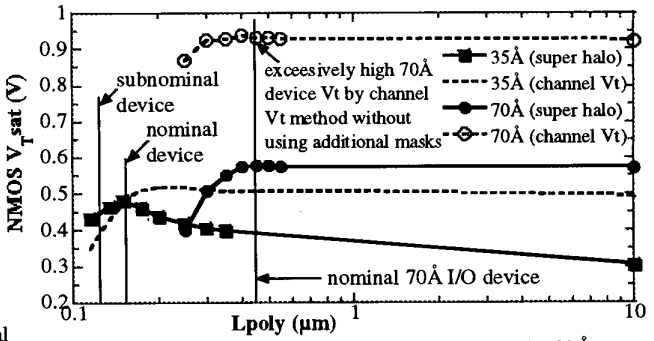

Fig.3 Super halo approach independently optimizes the 29Å or 35Å LL and 70Å I/O devices without using additional Vt masks. Much better short channel margin indicated by flatter Vt roll-off from nominal to sub-nominal gate lengths.

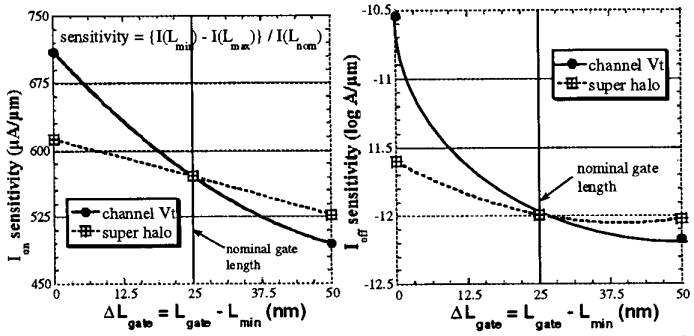

Fig.4 Super halo approach achieves less I_{off} and I_{on} sensitivity vs. gate length control (I_{on}: 15% vs. 38%; I_{off} in log[A/μm]: 3.5% vs. 13%) leading to tighter distribution of device characteristics for robust manufacturability.

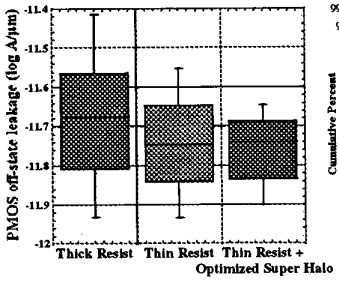

Fig.5 Device and process optimization reduces I_{off} and its spread by making shadowing effects negligible. Thus minimizes standby power.

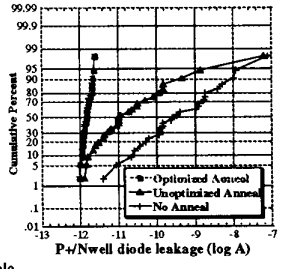

Fig.6 Optimized anneal reduces diode leakage, and PMOS narrow width effects by 40% (not shown). Thereby lowering SRAM I_{CC} leakage from 2.3 to 1pA/bit, resulting in lower standby power.

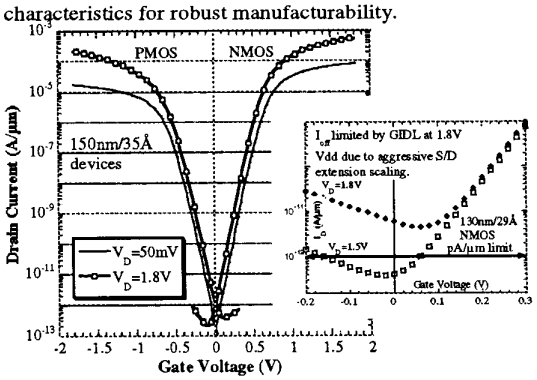

Fig.7 I_D-V_G characteristics after S/D extension optimization to avoid GIDL/BTBT limiting the device I_{off} especially when operating at 1.8V.

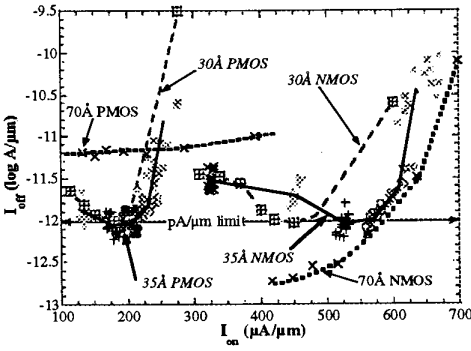

Fig.8 I_{on} vs. I_{off} curves for 70Å@3.3V, 35Å@1.8V and 29Å@1.5V devices show better performance than recently reported low leakage devices [5-7].

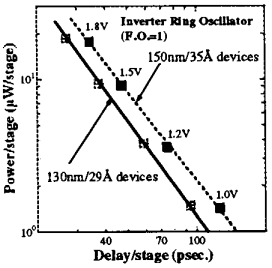

Fig.9 Power-delay trade off for both LL devices. Approximately 20% speed gain with 130nm/29Å devices at 1.8V or 45% reduction in dynamic power at 1.5V.

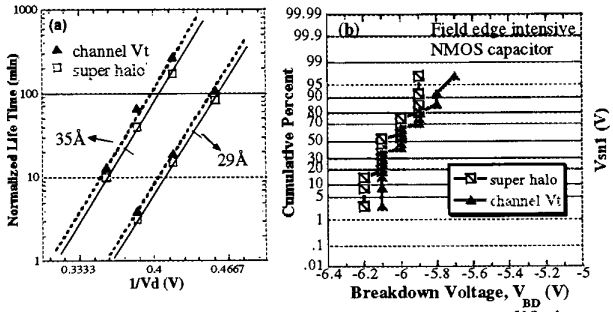

Fig.10 (a) Both types of devices show comparable HCI lifetime (within L_{poly}/wafer/lot variations), (b) Channel Vt devices exhibit worse V_{BD} due to channel boron/phosphorus out-diffusion to oxide.

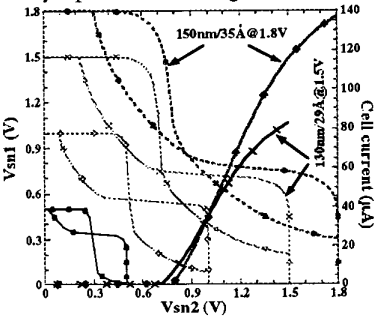

Fig.11 Functional butterfly curves of a 6T SRAM cell down to 0.5V. SNM is in excess of 350mV@1.8V.

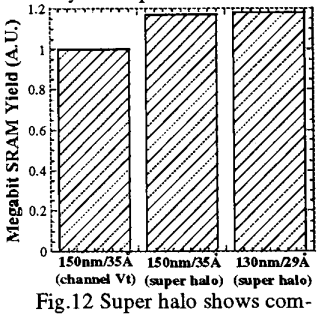

Fig.12 Super halo shows comparable or better SRAM yield. Equivalent yield also achieved by 130nm/29Å devices.