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A High Performance 3.97μm² CMOS SRAM Technology Using Self-Aligned Local Interconnect and Copper Interconnect Metallization

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ABSTRACT

In this work a 3.97μm² 6T CMOS SRAM bitcell technology has been developed using a logic based platform incorporating a self-aligned local interconnect and copper metallization. This 0.20μm process technology is suitable for stand-alone SRAM applications as well as embedded applications such as digital signal processors. A stable bitcell operation has been demonstrated for power supply (Vdd) of 1.8V. In this technology, the minimum transistor is (0.27μm X 0.15μm) with a gate pitch of 0.54μm and minimum metal pitch of 0.65μm.

INTRODUCTION

For workstation and server applications, a high performance SRAM is often required. As Vdd is scaled below 2.5V, the traditional 4T cell SRAM have shown a susceptibility to soft error and cell stability problems [1]. The need to meet increasing chip performance demands and low cost requirements of smaller bitcell dimensions merit the need to develop logic based SRAMs. We have developed a logic based SRAM with a bit cell area of 3.97μm² which features: shallow trench isolation, retrograde well, 0.36μm N+/P+ spacing, high performance logic MOSFET, Co-salicide, self-aligned local interconnect and copper metallization.

This integration uses dual Vt devices which distinguish the differences in the peripheral and array MOSFETS. The peripheral transistors use a N+ and P+ Co-salicide poly with low Vt (0.46 / -0.41V) to meet the high performance requirements. A capped polySi gate structure is used to form the array transistors. The Vt for the array NMOS and buried PMOS load device are optimized to provide good static noise margin and bitcell currents.

PROCESS INTEGRATION

In Figure 1 and Table 1 is the proposed SRAM cell layout with the process modular flow. To fabricate the 3.97μm² SRAM bitcell (1.80μm X 2.205μm), an aggressive N+ to P+ spacing of 0.36μm, retrograde well and self-aligned local interconnect module are required. Data from Figure 2 shows the N+/Nwell and P+/Pwell results with optimized photo and implant conditions. Optimizing the Nwell dose and implant settings enables a robust 0.36μm N+/P+ spacing. In fabricating the MOSFETs, a 35Å gate oxide is used with extensions and halo implants to provide good short channel behavior. A single mask integration, allows the fabrication of an in-laid self-aligned local interconnect module. An anti-reflective film is incorporated in the dielectric stack to optimize the printing characteristics of the local interconnect. Optical proximity correction (OPC) is utilized in the mask layout so that the DUV (248nm) lithography is able to print all features of the local interconnect layer [2]. The OPC of the LI mask and the anti-reflective layer allows printing of varying local interconnect aspect features which is critical to the formation of this module. The self-aligned local interconnect is defined by selectively etching the in-laid feature with respect to the etch stop layer. Figures [5-7] show an example of the OPC layout of the local interconnect, a top down SEM of the fabricated bitcell and cross sectional SEM after local interconnect formation. The self-aligned local interconnect module allows multi-functional uses such as a Vcc, Vss, bit line and cross couple contacts. The process is completed using a conventional copper metallization scheme which integrates with the proposed SRAM bitcell [3]. The completed integration is shown in Figure 8.

ELECTRICAL RESULTS

Figures 3 and 4 show the MOSFET IDS and Vt characteristics of both the peripheral and array devices. The use of Indium and Antimony to form the retrograde P well and N well respectively provide improved MOSFET rolloff characteristics. Table 2 shows a comparison of the MOSFET device requirements for both the peripheral and array devices. The in-laid Cu snake resistance is shown to range from 50- 65 m-ohm/sq. in Figure 9 for the nominal metal 2 linewidth of 0.36μm. Via resistance for the nominal 0.405μm X 0.405μm structure shows both the parametric chain and Kelvin structure to be less than 0.30 ohm/via (Figure 10). The in-laid copper metallization process provides this distinctive advantage as the via and metal fill occur concurrently during the deposition step. A second concern regarding the fabrication of the aggressive 6T SRAM bitcell is maintaining a balance between the static noise margin and bitcell current. The cell ratio for this bitcell is 1.0 with pass gate W/L = 0.27μm X 0.15μm and latch gate W/L = 0.27μm x 0.15μm. In this bitcell proposal we have achieved bit cell currents of 55-80uA for a 1.8V Vdd while maintaining the static noise margin in excess of 350mV (Figure 11 - 12).

CONCLUSIONS

A 1.8V high performance logic based SRAM technology has been developed and demonstrated on a 3.97μm² bitcell using a self-aligned local interconnect module with copper metallization. The development of this SRAM technology serves as an add-on module for the high performance logic platform and facilitates the re-use and consolidation of future SRAM and logic designs.

ACKNOWLEDGMENTS

The authors thank and acknowledge the collaborative efforts of our colleagues in the advanced design technology group in the test chip layout, Kevin Lucas for the OPC work, Bob Yeargain's logic process technology development and the support of the Advanced Products Research and Development Laboratory. The management support , from Fabio Pintchovski and Padmasree Warrior is greatly appreciated.

REFERENCES

1) C. Lage et al., IEDM 1996, p. 271
2) H. Chuang et al., IEDM 1997 p. 483
3) S. Venkatesan et al, IEDM 1997, p. 769

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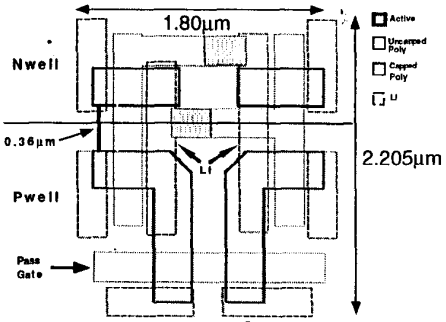

Figure 1: SRAM Cell - 3.97µm^2 (1.80 X 2.205)

Process Integration
o Shallow Trench
o Retrograde Well
o Dual Vt (Periphery / Array)
o Gate Oxide (35Å)
o Capped / Uncapped Gate
o Co-Salicide
o Self-Aligned Local Interconnect
o Contact
o In-Laid Copper Metallization
o Passivation

Table 1: Process Flow -"High Performance logic-based SRAM Process"

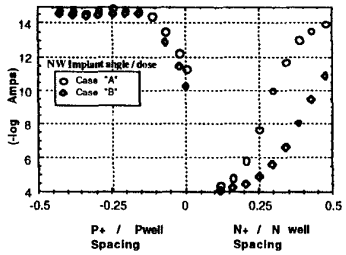

Figure 2: The P+ / Pwell and N+ / Nwell data shows the isolation is more robust for "case A".

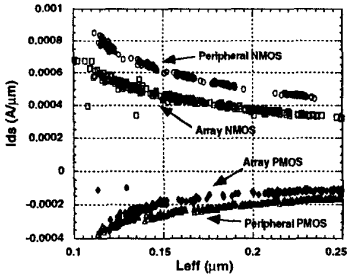

Figure 3: MOSFET IDS Transistor Characteristics

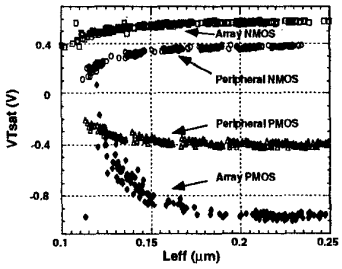

Figure 4: Vt behavior of NMOS / PMOS - The rolloff behavior with retrograde well shows less scatter in the Vt and better short channel behavior.

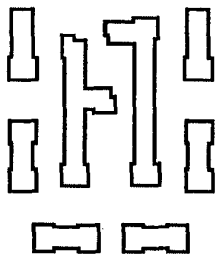

Figure 5: Example of using optical proximity correction applied to the local interconnect layer.

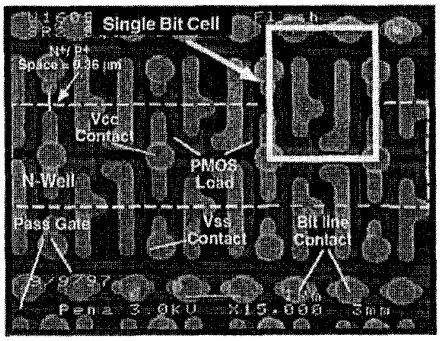

Figure 6: Top Down SEM shows the bitcell after contact CMP.

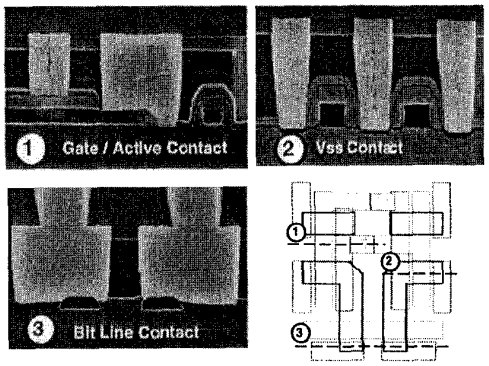

Figure 7: SEM cross section showing 3 applications in which the local interconnect is used in the the SRAM bitcell. A schematic diagram shows the area where the cross sections are taken.

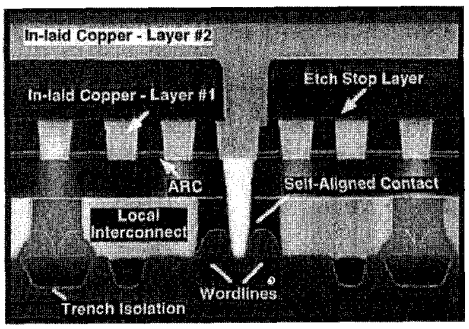

Figure 8: SEM cross section of logic based SRAM using enhanced local interconnect module and in-laid copper metallization

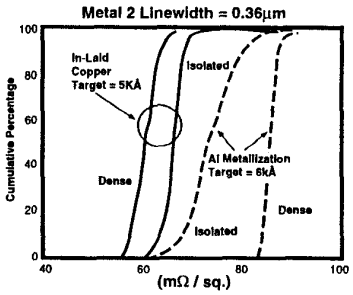

Figure 9: Snake interconnect resistance of in-laid copper and Al metallization.

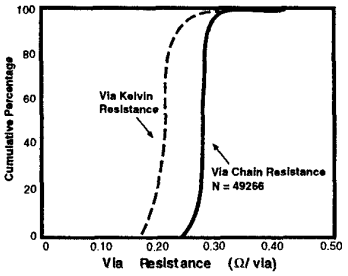

Figure 10: Via Resistance of In-Laid Copper Metallization. Nominal via size = 0.405µm X 0.405µm.

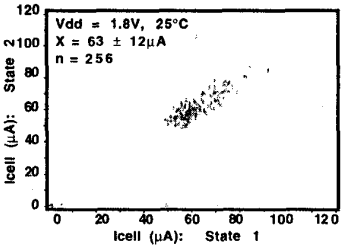

Figure 11: Bitcell current for both state 1 and state 2 of the 3.97µm^2 bitcell.

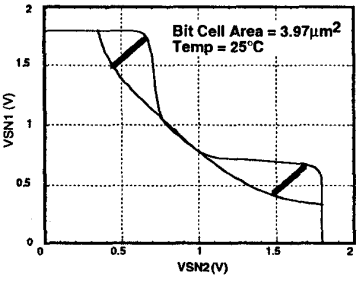

Figure 12: Butterfly curve of the bitcell. Static noise margin ranges from 350 - 400mV.

MOSFET Targets (@25°C)	IDS (µA/µm)	IL/W (Log Amps)	Vtsat (V)
Periphery			
NMOS	610	-10.5	0.46
PMOS	260	-10.5	-0.41
Array			
NMOS	400	-12	0.70
PMOS	100	-12	-0.95

Table 2: Nominal MOSFET device targets for peripheral and array devices.