A SUBMICRON, DOUBLE LEVEL METAL PROCESS

FOR HIGH DENSITY MEMORY APPLICATIONS

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Abstract

This paper will describe a process that was developed for application to a one megabit SRAM product. The minimum feature size of the Double Level Metal (DLM) process was 0.8 micron. Details relating to both metallization and to planarization will be discussed. The results of electrical characterization and reliability testing will be presented.

Introduction

The poor step coverage realized with sputtered metal and submicron contact diameters necessitated the move away from aluminum as interconnect. The material chosen for this process was Chemical Vapor Deposited (CVD) tungsten. Tungsten deposited in this fashion provides excellent step coverage and reasonable sheet resistance. For planarization an etched back Spin on Glass (SOG) process was developed. The use of SOG results in excellent topography smoothing without the need for complex equipment. Together, CVD tungsten and SOG are two of the key features of this high density, high volume, double level metal process. The lead design to utilize this process is a one megabit SRAM [1].

Process Technology

The conductor systems used in this process are CVD tungsten for metal-1 and aluminum alloy for metal-2. The tungsten is deposited in a semi-batch system which allows for high throughput. The rather high sheet resistance of 150 mohm/sq is not a problem in a BiCMOS type process where metal-1 is used for local interconnect. The adhesion of tungsten to oxide is typically poor, hence the need for an adhesion layer beneath the tungsten. The roughness of tungsten can cause alignment problems at the subsequent photolithography step. The solution to the rough texture is to lower the deposition temperature making the film more reflective. The patterning of the tungsten film is accomplished in a parallel plate, high pressure, single wafer etcher. The resultant etch profile is anisotropic with acceptable little etch bias (<0.1 micron). A SEM photo of a typical cross section is shown in Figure 1. The tungsten to oxide etchrate selectivity is 1.4:1 and the selectivity to photoresist is 2.5:1.

June 12-13, 1990 VMIC Conference
TH-0325-1/90/0000-0049 $01.00 C 1990 IEEE

The metal-2 layer is a sputtered film of aluminum-silicon-copper alloy. The resistivity of this film is important since major signal paths and power busses are routed using this layer. During the subsequent photolithography step reflective notching could be a problem if an antireflective coating were not used. For this reason a layer of titanium is sputter deposited on to the aluminum film. This not only reduces the reflectivity of the aluminum but also improves its electromigration resistance and reduces hillock growth. The grain size of the metal-2 layer is about 1.0 micron.

LEVEL	MATERIAL	RESISTANCE	PITCH
metal-1	CVD tungsten	150 mohm/sq	1.8 micron
metal-2	Al alloy	25	1.9

Topography smoothing is employed at two points in the process. The intermetal planarization process, the more complicated of the two, will be discussed next. The premetal-1 planarization is nearly identical and will not be discussed. The first step in the process is an undoped LPCVD oxide deposition. The is followed by two spins of siloxane SOG and then partial etchback of the SOG. This leaves SOG between metal-1 lines in densely packed areas and fillets along metal-1 lines in isolated regions. A second undoped LPCVD oxide deposition then encapsulates the SOG. Etchback selectivity of oxide to SOG and the amount of oxide removed to a large extent determine the degree of planarization. To characterize the SOG etchback an experiment was ran using Taguchi experimental design techniques. The parameters varied were; first oxide thickness, etchback selectivity and amount of oxide removed. Some results of this experiment are shown in Figure 2. The data indicate that increasing the oxide:SOG selectivity improves the planarization as shown by the decrease in metal-2 line resistance over topography. This is due to the change in selectivity at the microscopic level, otherwise known as the local loading effect [2]. Once oxygen is liberated from the deposited oxide during the etchback the SOG etchrate is increased. Thus, having a slow etchrate at the beginning of the etch improves planarization. The figure shows that increasing the first oxide thickness does not necessarily improve planarization. The results shown for increased etchback are not conclusive either. Typically, increases in etchback degrade planarization due to the local loading mentioned previously.

Electrical Characterization

The electrical results not described previously [3] will be discussed in this section. The resistance of CVD tungsten to heavily doped polysilicon and polycide is shown in Figure 3. The figure shows that contact resistance does not degrade for subdesign rule contacts. Specific contact resistivities are near 10 ohm-um2 and 2 ohm-um2 for doped polysilicon and polycide respectively. Aluminum metal-2 to tungsten metal-1 via resistance is also shown in Figure 3. Specific contact resistivity is about 0.2 ohm-um2.

It was found that by increasing the temperature of the CVD deposition the contact resistance could be made to decrease. Data from two experimental lots are shown in Figure 4. One possible explanation for this trend is that of an oxidized adhesion layer. Upon exposure to atmosphere the adhesion layer presumably oxidizes, which results in a poorly conducting layer between it and the CVD tungsten. It is unclear how increasing the deposition temperature would effect this oxidized layer. Another explanation is the interaction of the WF6 gas and the polysilicon. For this to occur WFx molecules would have to diffuse through the adhesion layer, either along grain boundaries or microdefects, and react with the polysilicon. This reaction would form poorly conducting compounds and consume some polysilicon. The effect of increasing the deposition temperature would be to increase the deposition rate thus limiting the time available for WF6/Si interaction.

Stacked contacts and vias can be implemented using this process. Typical resistances obtained when vias are stacked directly on contacts are 11ohm/stack (1 sigma = 6). This is slightly higher than the sum of the individual contact and via resistance values. Contact chain yields of this type of contact is around 80%. This result is for a chain of 790 stacked contacts where both contacts and vias are 0.8 micron in diameter.

Reliability

An integral part of interconnect process development is process reliability characterization. Electromigration (EM) testing has shown the aluminum metal-2 level to have good EM resistance. Figure 5 shows a lognormal plot of EM failure data for the stress conditions indicated. Extrapolation of the data to operating conditions yields less than 1 FIT after 20 years. Another method of evaluating conductor integrity is Breakdown Energy of Metal (BEM). This method has been used to evaluate the tungsten metal-1 layer. The BEM method is a rapid way of comparing sample metal to some baseline process. It is a fairly poor technique for comparison of different metal types, e.g. tungsten and aluminum.

Of emerging concern is the effect of interconnect processing on device performance. Of particular interest is transconductance degradation of MOS transistors due to hot electron trapping. Recent studies have shown a two orders of magnitude drop in lifetime due to intermetal planarization and metal-2 processing. The degradation is presumably caused by plasma processing which either effects gate oxide quality or generates species which passivate gate oxide defects. This is an area of intense study at the present.

Conclusion

It was shown that a highly reliable, very dense interconnect process was developed. Key features of the process include tungsten metal-1 and SOG etchback planarization. The tungsten metal layer provides excellent step coverage with good electromigration resistance. The tungsten patterning process results in very little etch bias and anisotropic etch profiles.

SOG planarization was shown to be dependent on both etchback selectivity between SOG and oxide and the length of etchback.

References

[1] B. Kertis et al., Symposium on VLSI Circuits, 1990 (to be presented).
[2] L. de Bruin et al., VMI-Conference Proceedings, p.404, 1988.
[3] W. Burger et al. IEDM Technical Digest, p.421, 1989.

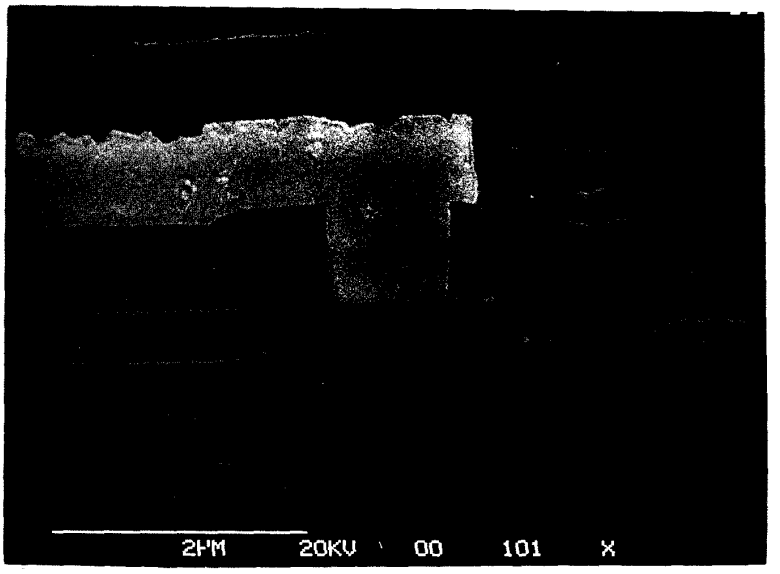

Figure 1. SEM cross-sectional photograph showing tungsten metal-1 contact to polysilicon.

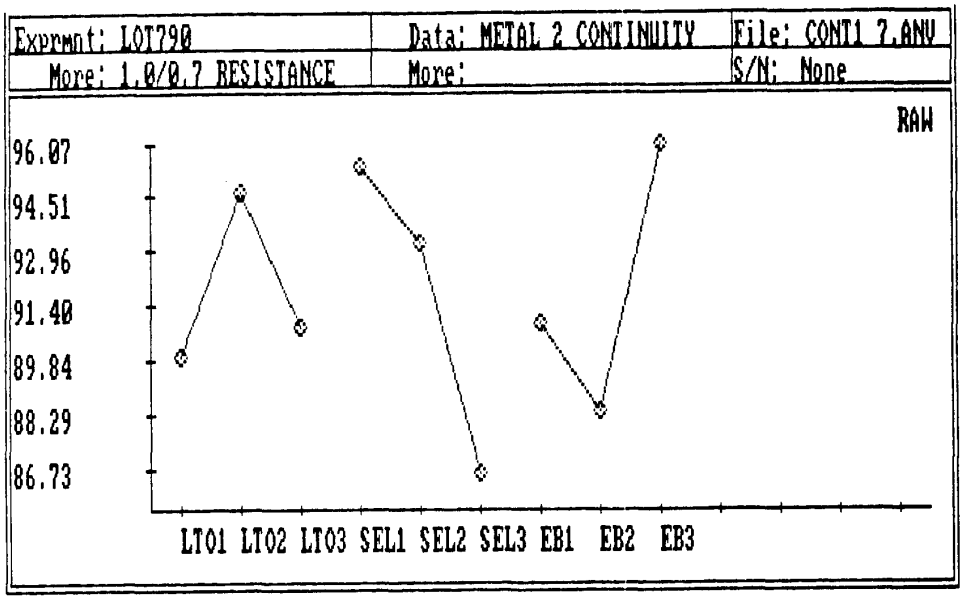

Figure 2. Results of Taguchi experiment on intermetal planarization and the effect on metal-2 continuity over topography: LTO (thin to thick), SELectivity (low to high), EtchBack amount (low to high).

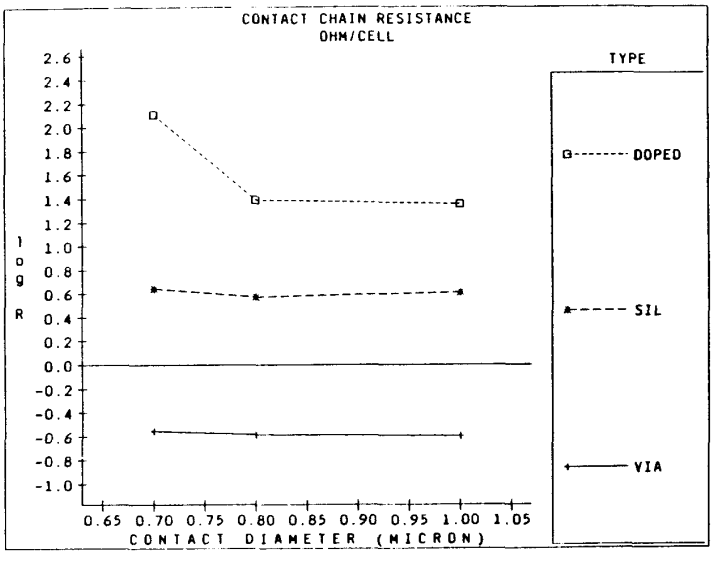

Figure 3. Contact resistances of tungsten metal-1 to doped polysilicon, polycide and aluminum metal-2.

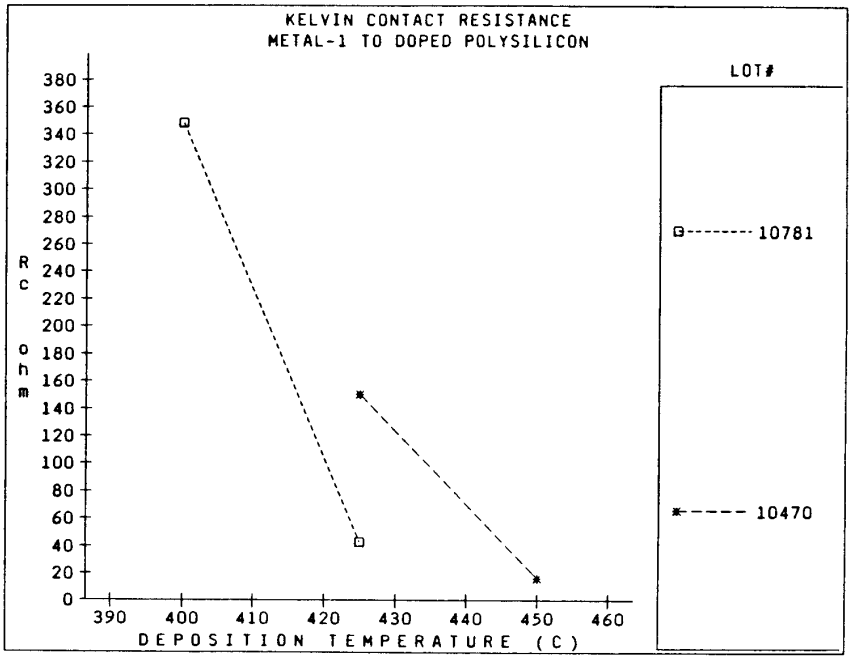

Figure 4. Tungsten metal-1 to doped poly contact resistance as a function of CVD tungsten deposition temperature.

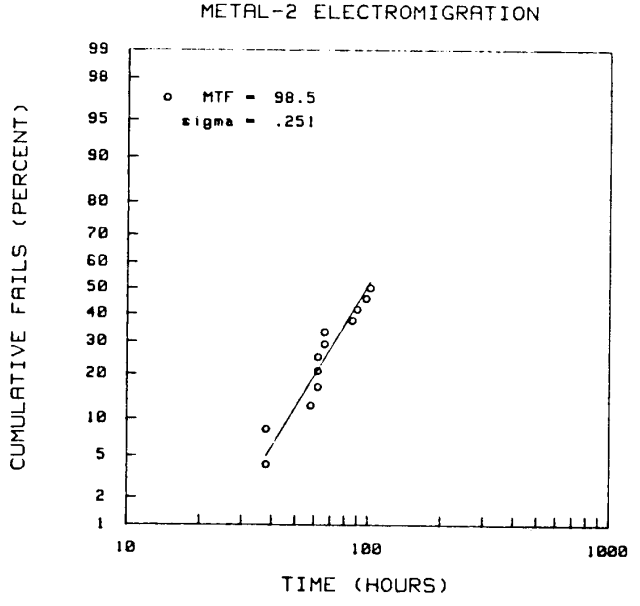

Figure 5. Lognormal plot of electromigration failure data for Al metal-2. Stress conditions: J=1.6A/cm2, T=233C.