Tailoring Interfacial Oxide for Polysilicon Bit-Cell Contacts and Emitters with In Situ Vapor HF Interface Cleaning and Polysilicon Deposition in a 4Mbit BiCMOS Fast Static RAM

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Abstract -- A cluster tool based technique for in situ vapor HF cleaning, ultra thin oxide growth and polysilicon deposition is compared to conventional processing in forming polysilicon emitters and polysilicon bit-cell contacts in a 4Mbit/0.5um BiCMOS FSRAM process. Results are reported which indicate that the control achieved with cluster tool processing provides greater flexibility in simultaneously optimizing the performance of both the polysilicon emitters and bit-cell contacts.

I. Introduction

As the need for fast and high density static RAMs increases to support advanced microprocessors, the designers of fast static RAMs (FSRAMs) are frequently embracing BiCMOS methodologies to meet the access time requirements for memories at the 4Mbit level and beyond. For this application many familiar aspects of polysilicon bipolar device fabrication must be rationalized in terms of the total device fabrication process when defining a BiCMOS technology.

While high performance bipolar devices provide techniques for achieving fast access times in BiCMOS FSRAMs, self-aligned polysilicon bit-cell contacts provide one of the techniques for achieving a small bit-cell size at the 4Mbit density level. In one bit-cell design the Vss supply voltage is brought into the memory cell without a traditional metal contact. The Vss bus, which is routed over the cell in second level polysilicon, is connected to the area between each pair of pull-down gates through a self-aligned bit-cell contact. The contact area between second level polysilicon and N+ substrate can be as small as 0.6um x 0.2um when permanent gate sidewall spacers are used. The structure of the bit-cell contact is depicted in an SEM cross section in Fig. 1.

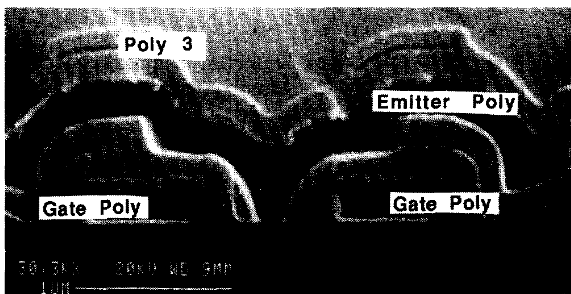

Fig 1. A cross-sectional SEM photograph of a 0.5um Poly 2 to substrate contact self-aligned between two pull-down gates.

The aspect ratio and small dimensions of these contacts can make removal of native oxide difficult with conventional wet etching techniques.

In this paper we describe in situ processing techniques which involve removing native oxide with vapor HF, optionally growing several monolayers of thermal interfacial oxide and depositing a polysilicon film using a load locked multi-chamber cluster tool. We have examined the the capability of this process to produce low bit-cell contact resistance while tailoring bipolar gain through the use of a thin interfacial oxide. The results achieved in satisfying these competing requirements are reported.

II. Processing

The process used to produce the circuits and test structures described in this work is described in [1]. The sequence to form the bit-cell contact and polysilicon emitter is:

- Etch Openings in Poly 1 to Poly 2 Dielectric
- Pre-Poly 2 Deposition Clean
- Poly 2 Deposition
- Poly 2 Doping (Implant)
- Poly 2 Anneal

While it is possible to produce thinner interfacial oxides with the in situ process described above, a target of 10Å of interfacial oxide was selected for the in situ oxide examined in this work. Subsequent processing capable of producing interfacial oxide breakup includes a short 1050°C Rapid Thermal Anneal (RTA) after second polysilicon doping and a similar anneal before contact etch for doped glass planarization.

To distinguish the three processes we will compare in this work we identify the following: 1)--a traditional wet HF pre-clean and polysilicon deposition process, the "Wet HF Pre-Clean" process; 2)--an in situ vapor HF pre-clean/poly deposition process targeted to producing a minimum of interfacial oxide, the "Oxide Free" process; and 3)--an in situ vapor HF pre-clean/oxidation/poly deposition process targeted to produce a controlled oxide at the polysilicon interface, the "Controlled Oxide" process. In situ processing was accomplished in an ASM vertical reactor cluster tool, the Advance 600/2.

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Cross-section TEM imaging was used to observe and evaluate the interfaces produced by each of the three processes. The micrographs obtained are shown in Figs. 2a, b, and c. Significant observations from these TEMs are summarized in table I.

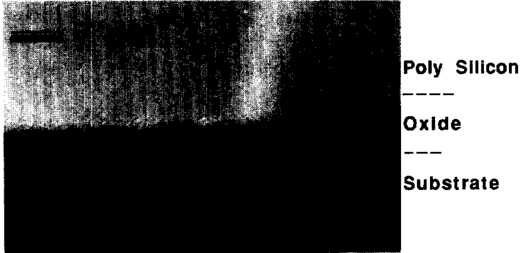

Fig 2a. TEM photo of "Wet HF Pre-Clean" poly interface.

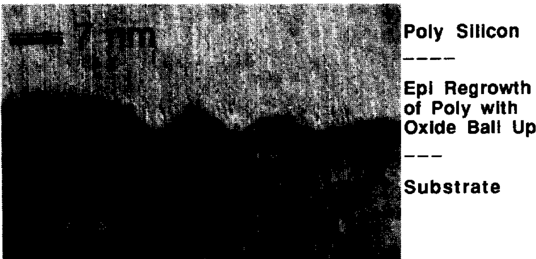

Fig 2b. TEM photo of "Oxide Free" poly interface.

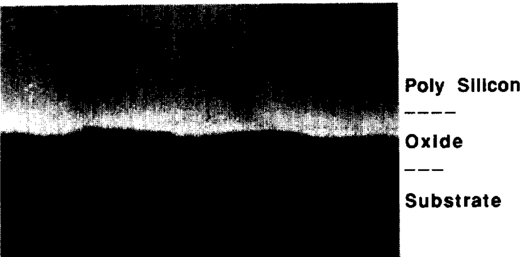

Fig 2c. TEM photo of "Controlled Oxide" poly interface.

TABLE I
TEM OBSERVATIONS OF EMITTER INTERFACE CHARACTERISTICS

Emitter Poly Pre-Clean Process	Oxide Thickness in Å	Epitaxial Regrowth
Wet HF Pre-Clean	20-25 Å	None
Oxide Free Process	8-10 Å	Regrowth Observed
Controlled Oxide Process	18-20 Å	None

A very thin and largely discontinuous interfacial oxide is seen with the "oxide free" process. In contrast, a significant oxide is present with both the "wet HF" and the "controlled oxide" process. Epitaxial regrowth of the polysilicon layer, which is suppressed by residual interfacial oxide, was observed after RTA anneal with the "oxide free" cluster tool process but not with either the "wet HF" or the "controlled oxide" process.

III. Contact Resistance

Bit-cell contact resistance (Rc), measured with Kelvin contacted structures, is plotted versus inverse contact area in Fig 3. Significantly higher contact resistance values are measured when an in situ interfacial oxide process is used than when either the "oxide free" or the conventional "wet HF" clean processes are used.

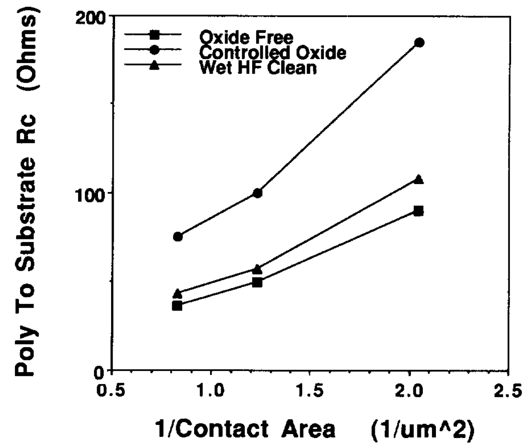

Fig 3. Bit-cell contact resistance between emitter poly and substrate is plotted against the reciprocal of contact area.

A strong radial variation in Rc is observed with the "wet HF" process while only a weak front to back dependence is seen with the "oxide free" process. A larger front to back variation in Rc is seen with the "controlled oxide" process. See Fig 4a, b, and c (last page-same vertical scale on all plots).

IV. Polysilicon Emitter Transistor Characteristics

The emitter resistance is significantly lower and H_{FE} roll-off is pushed out to higher emitter currents with the "oxide free" process. This is reflected in higher emitter knee current values. Emitter resistance (R_E) and knee current (I_{KE}-the emitter current for a 10% roll-off in H_{FE} from peak H_{FE}) are given in Table II.

TABLE II
POLYSILICON EMITTER INTERFACE RELATED BIPOLAR DEVICE PARAMETERS BY POLYSILICON DEPOSITION PROCESS FOR A 0.8umx2.4um EMITTER

Process	R_E	I_{KE}
Oxide Free	18.0 ohms	3.4 mA
Controlled Oxide	23.6 ohms	2.9 mA
Wet HF Pre-Clean	20.4 ohms	2.5mA

Comparing the normalized H_{FE} roll-off across process groups in Fig. 5 we note improved high current H_{FE} roll-off with the "oxide free" emitter process.

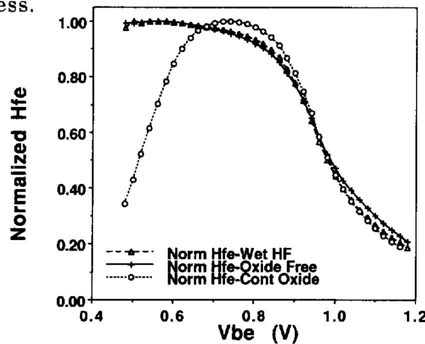

Fig 5. Normalized H_{FE} versus V_{BE} by polysilicon emitter deposition process. Peak H_{FE} has been normalized to 1.0.

In comparing the distributions of peak H_{FE} values for the "oxide free", the "controlled oxide" and the "wet HF" clean processes in Fig. 5., we observe the "oxide free" process produces a much lower and more tightly controlled H_{FE} distribution than either the "controlled oxide" or the conventional "wet HF" clean process.

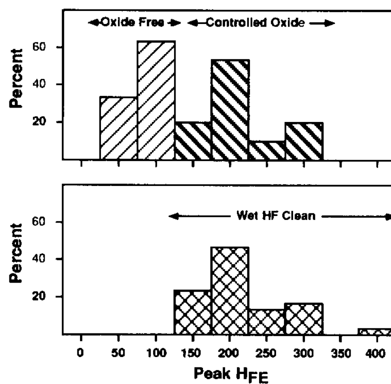

Fig 6. Peak H_{FE} distributions by polysilicon emitter deposition process. Upper left--"oxide free" in situ clean process, upper right--"controlled oxide" in situ clean and oxidation process and bottom distribution--conventional "wet HF" clean and polysilicon deposition.

While the collector currents are very similar for all three processes, the "oxide free" process produces significantly higher base current and lower H_{FE}; see the Gummel plots in Fig 4. below.

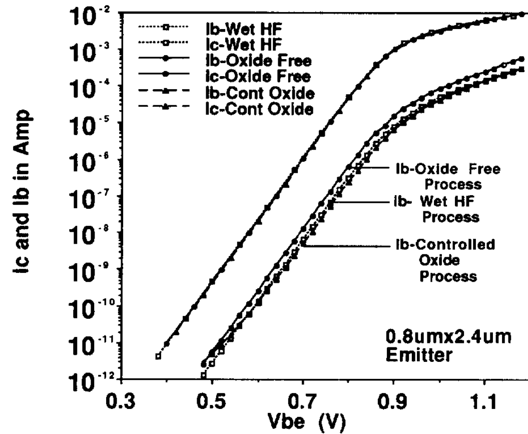

Fig 7. Ic and Ib versus Vbe for 0.8umx2.4um n-p-n devices by emitter poly deposition process.

Average H_{FE}, average base saturation current (I_{Bsat}) and average collector saturation current (I_{Csat}) are summarized in table III by emitter poly deposition process. The differences in H_{FE} among groups are directly related to the higher I_{Bsat} seen with the "oxide free" emitter process. By adjusting the thickness of the oxide barrier at the emitter interface, we are able to tailor critical bipolar device characteristics.

TABLE III
PEAK H_{FE}, BASE AND COLLECTOR SATURATION CURRENTS BY POLYSILICON DEPOSITION PROCESS

Process	Peak H_{FE}	I_{Bsat} (A/um^2)	I_{Csat} (A/um^2)
Oxide Free	79	0.77×10^{-20}	0.78×10^{-18}
Controlled Oxide	231	0.28×10^{-20}	0.76×10^{-18}
Wet HF Pre-clean	236	0.36×10^{-20}	1.57×10^{-18}

V. Conclusions

We have compared two integrated pre-clean/polysilicon deposition processes which provide

for direct control of interfacial oxide to each other and to a conventional "wet HF" clean and polysilicon deposition process. The "oxide free" process has provided reduced bit-cell contact resistance and improved H_{FE} control while the "controlled oxide" process increases H_{FE}. The ability to tailor interfacial oxide between poly and single crystal silicon provides the flexibility to optimize the emitter poly deposition to suit the circuit requirements of a specific BiCMOS process.

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REFERENCES

[1] J. Hayden et al., IEEE Trans. Electron Devices, vol. 39, pp 1669-1679, July 1992.

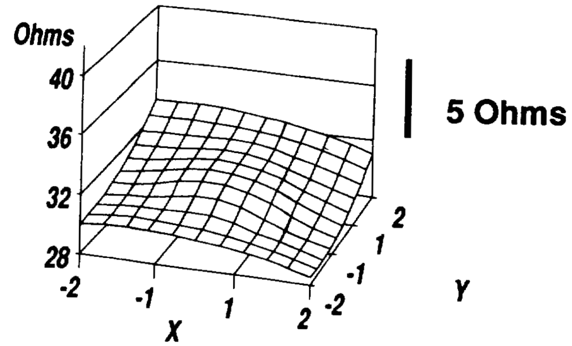

Fig 4b. Topological display of Rc over wafer surface for "oxide free" process.

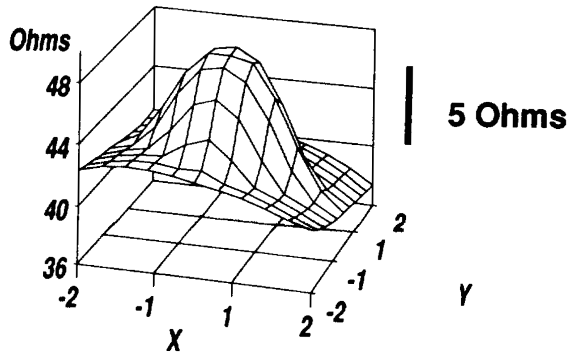

Fig 4a. Topological display of Rc over wafer surface for "wet HF" process.

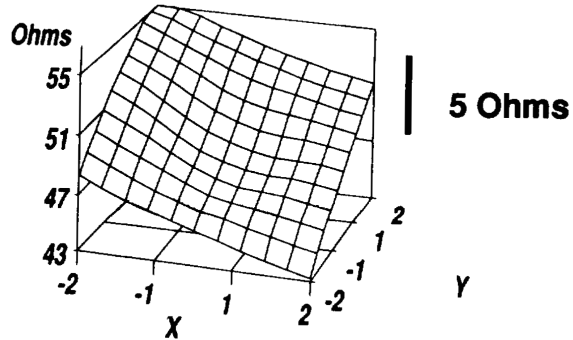

Fig 4c. Topological display of Rc over wafer surface for "controlled oxide" process.