The SCC BJT: A High-Performance Bipolar Transistor Compatible with High-Density Deep-Submicrometer BiCMOS SRAM Technologies

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Abstract— **We present the process development and device characterization of the Selectively Compensated Collector (SCC) BJT specifically designed for high-density deep-submicrometer BiCMOS SRAM technologies. This double-poly BJT takes advantage of the self-aligned polysilicon layers of the SRAM bit cell to obtain high performance without adding excessive process complexity. Furthermore, although an NPN device, the SCC BJT is formed in a lightly doped p-well in which the collector is formed with a single 370 keV phosphorus implant to minimize parasitic junction capacitances without the use of trench isolation or recessed oxides. The suitability of this bipolar structure outside of its original FSRAM intent is proven with its potential for bipolar logic and mixed-mode RF applications. ECL delays of 50 ps at 200 μA and a CML power-delay product of 4.5 fJ at 1.1 V supply were obtained. A 900 MHz noise figure as low as 0.54 dB at 0.5 mA with an associated gain of 14.7 dB was demonstrated as well as a dual modulus ÷ 4/5 prescaler operating up to 3.3 GHz for a switch current of 200 μA.**

I. Introduction

In the past decade, the evolution of the silicon Bipolar Junction Transistor (BJT) for digital integrated circuit applications split into two parallel efforts. The first was the continued optimization of bipolar-only technologies for use in very high-speed systems. The second was the merging of bipolar and CMOS into a single BiCMOS technology.

High-performance bipolar-only technologies used sophisticated double-poly self-aligned base-emitter structures with deep trench isolation; see e.g., [1]–[5]. Recent advances in silicon-germanium technology allowed the use of Ge_xSi_{1-x} strained layers in the base region of bipolar transistors leading to impressive bipolar-only technologies [6], [7]. However, these latter Ge_xSi_{1-x}/Si technologies have not found wide applications because the added complexity of Ge_xSi_{1-x}/Si did not yield sufficient return at the digital systems level and because bipolar-only technologies were not able to compete with the continued scaling-down of CMOS device size and power.

BiCMOS technologies generated enthusiasm because they promised the density and low power of CMOS, but the speed of bipolar when applied only to critical paths. However, microprocessors continued to use CMOS because their rapid circuit evolution, complexity, and bus-width made the selective use of bipolars difficult. DRAM's and commodity SRAM's were density—not speed—driven, thus the additional bipolar cost was not justified.

The only place digital BiCMOS technologies found significant application was in Fast Static RAM's (FSRAM's), where a "good enough" bipolar bought sufficient reductions in memory access time, that the cost of a complex bipolar structure was not justified. Recently, however, the increased speed requirements of FSRAM's motivated us to design a high-performance bipolar device, the Selectively Compensated Collector (SCC) BJT, in a high-density 0.35 μm BiCMOS technology which now meets the performance of many complex bipolar-only technologies. The SCC BJT formation and characterization will be discussed in the next sections. Like other successful FSRAM BiCMOS technologies, we attempted to minimize the device complexity, while obtaining high performance through a nonconventional well structure and base formation. The low complexity and high performance of the SCC BJT enables the 0.35 μm BiCMOS technology to find applications far outside its initial FSRAM intent, including mixed-mode bipolar RF and high-speed bipolar ECL/CML circuits.

II. The SCC BJT: Overview

The bipolar module added to the core CMOS process consists of only 5–6 non-critical implant masks, epi, and an ~1100°C, 20 second RTA. No deep trench, shallow trench, or recessed isolation is added. Neither are selective epi or sophisticated base contact structures introduced. Despite this, the bipolar performance is near state-of-the-art, with only one major disadvantage—the lower packing density of junction isolated bipolar devices, resulting in a $\sim 10 \times 10\ \mu m^2$ footprint.

Described next are the SCC BJT structure and associated process issues, starting with the well and following sequentially to the base and then the emitter formation.

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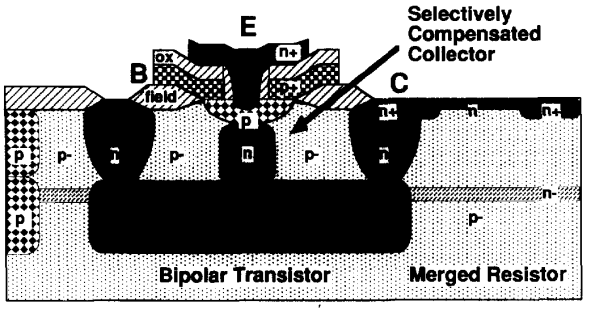

Fig. 1. Cross-sectional drawing of the double-poly SCC BJT formed in a lightly doped p-well. The polysilicon emitter (E) and base (B) electrodes are indicated, as is the collector contact (C). The p-well also provides low junction capacitance for the diffused ECL load resistor.

III. The SCC BJT: Well Formation

Fig. 1 shows a cross-sectional drawing of the double-poly SCC BJT. An n+ buried layer followed by epitaxial silicon growth is required to obtain a low collector resistance and limit the Kirk (base push-out) effect. A p buried layer is required for isolation between adjacent n+ buried layers. As shown, the n+ and p buried layers are set in a p-substrate, and are not self-aligned to allow minimizing the collector to substrate capacitance with a buried layer offset.

For the 0.35 μm generation, the PMOS n well ($\sim 2 \times 10^{17}/\text{cm}^3$) and bipolar n well ($\sim 5 \times 10^{16}/\text{cm}^3$) doping requirements have diverged sufficiently that they can no longer share a common well. Rather than mask a separate bipolar well implant, the SCC structure combines a 370 keV phosphorus self-aligned collector implant with the masked active base implant, to fully set the collector doping with a single high-energy implant. This technique, when used to augment the collector doping, is often referred to as a pedestal or SIC implant [1]. In our case, the bipolar epi-region (1.6 μm thick, as grown) over the n+ buried layer is lightly p-doped (to $\sim 1 \times 10^{15}$ cm^{-3}), so that the collector implant is actually compensating; see Fig. 1. Since this SCC implant uses the base implant mask, it is self-aligned to the emitter (which is outdiffused from a subsequently deposited second layer of polysilicon) by the p+ poly base electrode. The advantage of the lightly doped epi-region includes not only a lower value of C_{BC}, but also a lower value of C_{CS} without the need for deep trench or recessed oxide isolations. Also, as shown, the substrate capacitance of the n diffusion resistors can be kept very low (<1 fF for a 2.4 μm $\times$ 1.6 μm resistor at 3 V bias) by using n-type diffusions in this same p-substrate.

Although the SCC BJT has a reduced value of C_{BC} by localizing the active collector region directly below the emitter, there is a drawback to this structure, as seen in Fig. 2. Shown is a PISCES-II [8] simulation of electron concentration as a function of position through the npn BJT with a 0.60 μm wide selective collector implant. The confinement of electron density (and current) to the region of high collector doping inhibits the 2-D spread of electron current as it approaches the n+ buried layer. This increases the collector resistance and the susceptibility to the Kirk effect. Fig. 3 shows the effect this has on the unity current-gain frequency, f_T, at high

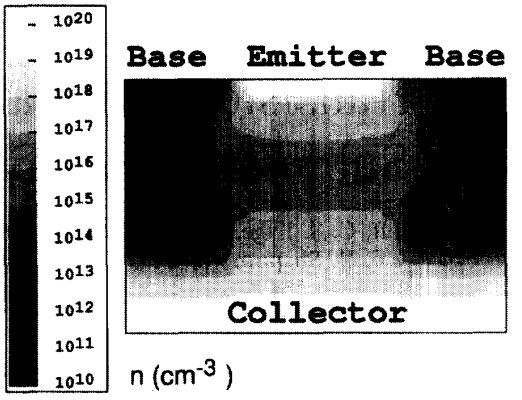

Fig. 2. PISCES-II simulations of electron concentration as a function of position through the npn BJT with a 0.60 μm wide selective collector implant. $V_{\text{CE}} = 2.0$ V, $V_{\text{BE}} = 1.0$ V, and $J_C = 7.6 \times 10^{-4}$ A/μm. Note the confinement of electron density (and current) to the region of high collector doping.

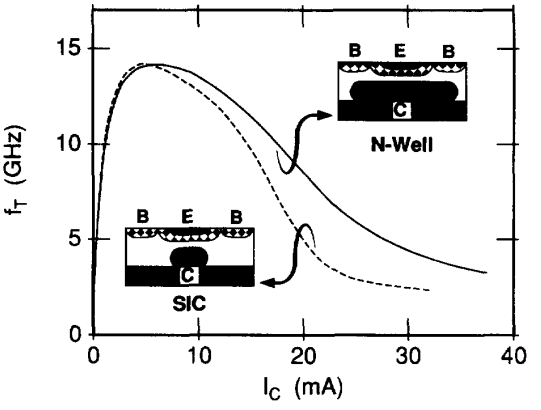

Fig. 3. Representative measurement of the unity current-gain frequency, f_T, as a function of collector current extracted from s-parameter measurements on 0.8 μm by 20 μm transistors.

currents. Shown is the measured f_T of two identically-formed bipolar transistors with differing collector widths, reported in an earlier study [9]. Although the peak values of f_T agree within experimental error, the high-current behavior of the SCC transistor is inferior. Further two-dimensional device simulations indicated, moreover, that for realistic loads of 0.1 pF/μm, that the voltage response of the the SCC BJT is only $\sim$3% slower.

Setting the collector doping fully with the SCC implant in a nonself-aligned "CMOS twin-well" process saves one masking step; however, a localized collector does not provide isolation between the base and substrate, which would be obtained with a wider n well or a deep trench. In the SCC BJT, this isolation is obtained by fully encompassing the active area of the bipolar transistor with the n+ deep collector (or reach-through) diffusion, as in [10]; see Figs. 1 and 4.

IV. Effect of Arsenic Autodoping

Arsenic was used for the n+ buried layer because of its low diffusivity, low defect generation rate, and high solid sol-

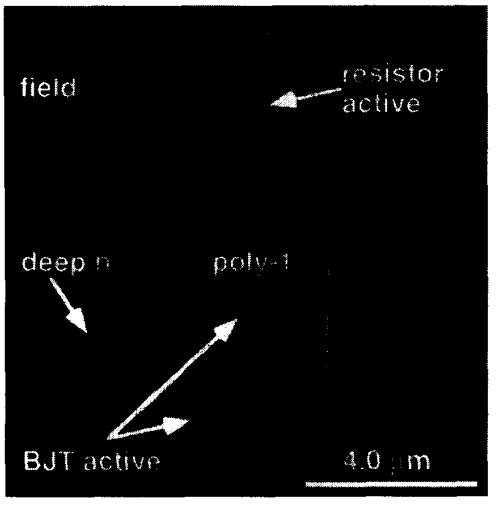

Fig. 4. Tilt-angle SEM after poly-1 etch, showing how the deep n+ implant into the BJT's outside active ring isolates the base and substrate in addition to reducing the collector resistance.

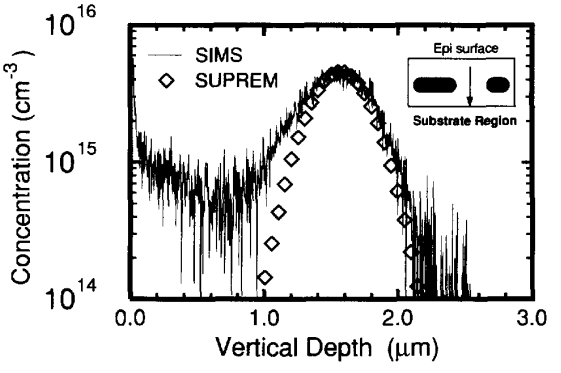

Fig. 5. SIMS profile of arsenic concentration through a substrate region to characterize arsenic autodoping. 1.5 μm of intrinsic epi was grown on patterned n+ buried layers, and subsequently annealed.The SUPREM-III simulation of this same anneal place a dopant spike at the epi-substrate interface using the measured arsenic sheet density, 2.5 $\times$ 10^{11}/cm^2.

ubility. As a drawback, arsenic's high vapor pressure leads to significant autodoping; see Fig. 5. The as-ingrown autodoping shows a fairly abrupt peak, which broadens during subsequent thermal processing. The presence of this n-type layer can increase the size of the offset n+ buried layer, significantly increasing C_{CS}; see Fig. 1.

Complete reduction of the buried autodoping spike is not required, however. First, this dopant spike is compensated by the p dopants in the substrate and epi. Second, even if a slight net electron sheet remains at the epi-substrate interface at zero bias, it is depleted under reverse bias. See Fig. 6, which shows PISCES II simulations of electron and hole concentrations for a 3 μm deep collector offset from a 3 μm deep p well. The p well's great depth results from it merging with the p buried layer. The n-type autodoping sheet density for these simulations is the same as measured in Fig. 5.

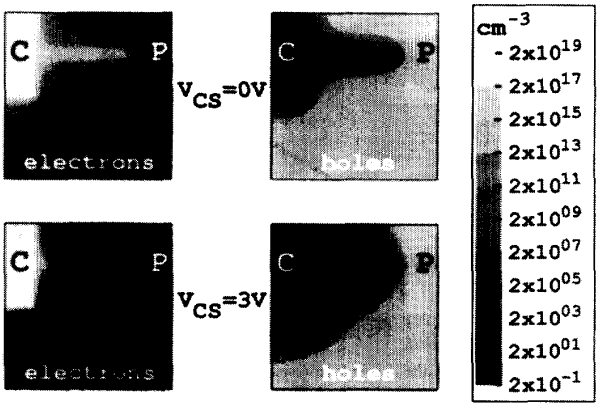

Fig. 6. PISCES II [8] simulations of electron and hole concentrations for a 3 μm deep collector offset from a 3 μm deep p well. The substrate and offset are p-doped, 7 $\times$ 10^{14} /cm^3. The n-autodoping spike has a sheet density of 2.5 $\times$ 10^{11} /cm^2.

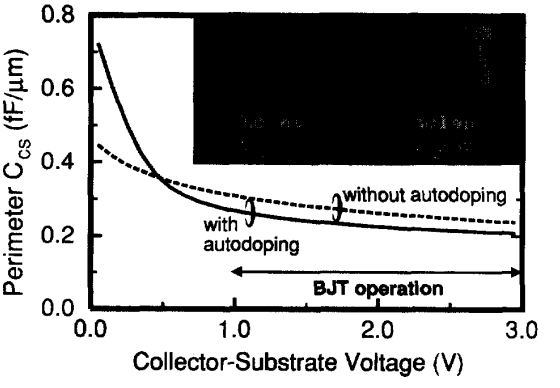

Fig. 7. Simulated collector-periphery junction capacitance for the structure of Fig. 6 as a function of reverse bias (with autodoping). As a comparison, the simulation was repeated for the same structure without autodoping, with the associated hole concentration plots shown as inserts.

Fig. 7 shows the simulated collector-periphery junction capacitance for the structure of Fig. 6 as a function of reverse bias. Note the rapid drop in capacitance until the electron concentration of the autodoping spike is fully depleted. Once this has occurred, the built in field acts to extend the depletion region further than if there were no autodoping. The periphery capacitance for the case of no autodoping is plotted as a comparison, and the hole concentration shown as an insert in Fig. 7. Note that though moderate amounts of autodoping increase the zero-bias value of C_{CS}, the value of C_{CS} under active bias is actually *decreased.*

One other concern is the effect that autodoping has on the linearity of the n diffusion resistor targeted at 1600 $\Omega/\square$, since the n-type autodoping can act as a shunt path, see Fig. 1. The measured variation in resistance is actually under 2%, and the mechanism responsible is not a parallel shunt path, but rather an increasing resistance with bias due to depletion, even by the lightly doped p-well. Fig. 8 shows that the mismatch between discrete and merged resistors is also under 2%. Finally, these diffusion resistors show excellent temperature stability, with their values shifting $\ll 0.1\%/°C$.

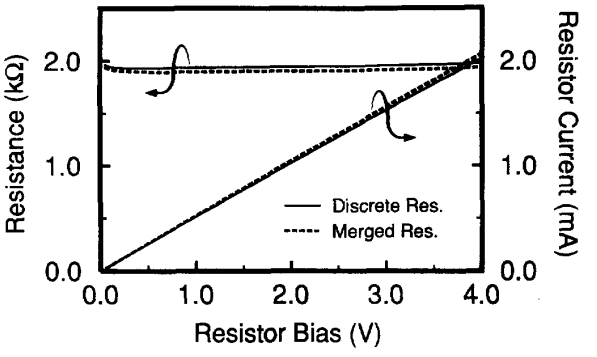

Fig. 8. Linearity of the n diffusion resistor placed in the p-bipolar well. The resistor current and resistance for both a discrete and a merged resistor are shown. The latter has a 1.5% lower resistance.

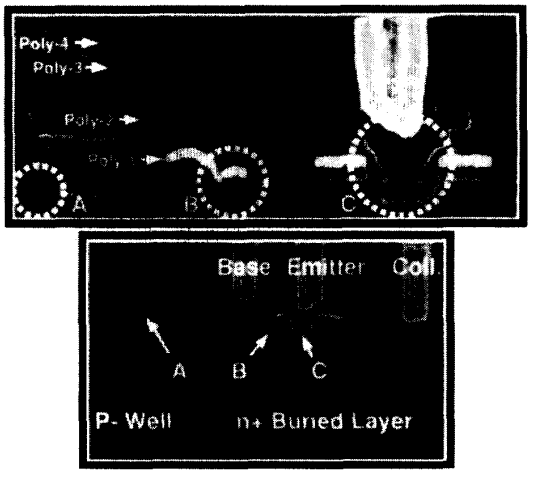

Fig. 9. Cross-sectional SEM of the 0.35 μm BiCMOS SRAM bitcell (above) showing the four layers of polysilicon which enable a dense 6-T memory cell using TFT's.The LOCOS isolation (A) and first two layers of poly form the bipolar transistor (below). Buried contacts (B) and (C) of the bit cell are the base and emitter contact of the BJT.

V. SCC BJT-SRAM Bit Cell Synergism

The following sections focus on the formation of the self-aligned emitter-base contacts. Fig. 9 contrasts a cross-sectional SEM of the 0.35 μm BiCMOS SRAM bit cell with that of the SCC BJT. The 0.35 μm BiCMOS technology was constrained by a dense bit cell design, requiring four layers of polysilicon. The first layer of polysilicon forms the MOS transistors, the second forms a self-aligned landing pad for the bit line contact and supplies V_{SS} to the memory array. The third and fourth layers of polysilicon form the p-channel TFT, stacked vertically above the substrate.

To prevent excessive process complexity, the addition of the NPN BJT relied on the first two existing polysilicon layers, both of which were strapped with polycide to reduce their sheet and metal-contact resistance. Poly-1 strapped with WSi, which forms the MOSFET gate, also forms the extrinsic base using the existing buried contact of the bit cell, and poly-2 strapped with TiSi forms the emitter using the self-aligned bit line poly-2 contact; see contacts (B) and (C) in Fig. 1. Further details of the 0.35 μm BiCMOS technology are given in [11].

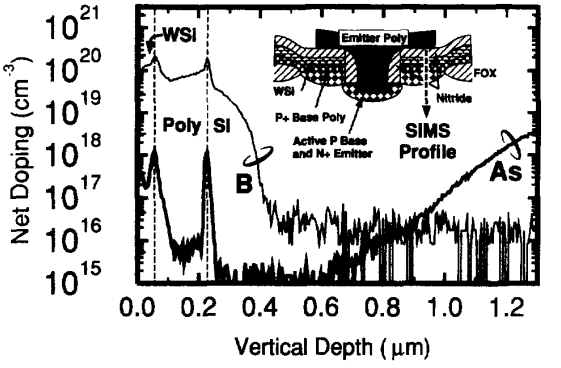

Fig. 10. SIMS profile of boron (B) and arsenic (As) through the extrinsic base region of the NPN BJT, as indicated by the insert.

VI. Base Formation

As shown by the insert of Fig. 10, p+ polysilicon strapped with tungsten polycide and a nitride dielectric cap is used as a self-aligned connection to the active base of the bipolar transistor. During the overetch of this electrode, the exposed active silicon region of the bipolar transistor is recessed or "trenched." The link-up to the active base is obtained by the extrinsic base region, formed by outdiffusion from the polysilicon base electrode. The SIMS plot shows a vertical depth of the extrinsic base region of ~0.18 μm. As in [12], we found that WSi is not a good diffusion source for boron, and implanted the boron into the polysilicon prior to WSi polycide deposition.

It is important to place the peak of this masked implant near the poly-to-silicon interface, thus ensuring formation of the extrinsic base region despite segregation of boron to the WSi interfaces. See Fig. 10, where the concentration gradient shows boron diffusion from the poly into the WSi. Integration with the CMOS flow introduces two impediments which further justify this "brute-force" extrinsic base formation. First is the existence of a thin chemical oxide layer between the polysilicon and the silicon substrate, resulting from a defect-reducing clean which leaves the surfaces hydrophilic. The oxide layer increases the contact resistance and retards the boron outdiffusion required to form the extrinsic base region. Second, the primary thermal cycle used to drive out boron from the base electrode is an RTA of ~1100°C for 20 seconds used to activate the emitter. The shallow junction requirements of the 0.35 μm CMOS devices do not allow a longer or hotter emitter anneal.

VII. Base Resistance Sensitivity

The electrical data presented here is for a 1200 Å nitride, 1000 Å WSi, and 550 Å p+ poly base electrode stack, with a p+ poly implant dose of $5 \times 10^{15}/\text{cm}^2$. The table insert shown in Fig. 11 shows the strong dependence the extrinsic base junction depth has on the p+ poly implant range, where BF_2 was used to obtain very short ranges. Reduction of the boron implant range into the polysilicon not only greatly reduces the extrinsic base formation, but also drives the poly-to-silicon contact resistance to unacceptably large values. These

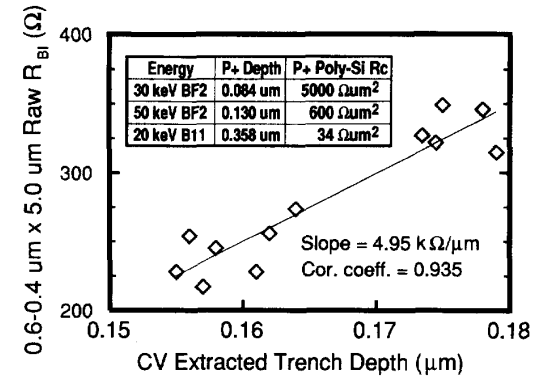

Fig. 11. Table insert shows extrinsic base depth below the poly-to-silicon interfaceand corresponding contact resistance of this interface as a function ofimplant energy for a dose of $5 \times 10^{15}/\text{cm}^2$. Plot shows intrinsic base resistance versus active area silicon trenching.

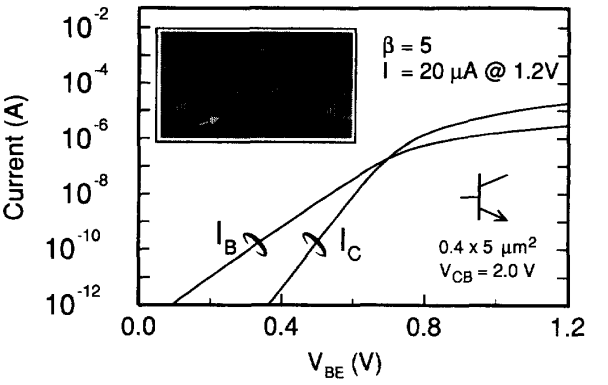

Fig. 13. Characteristic Gummel plot for a BJT with insufficient dopant diffusion from the implanted poly-2 surface to the substrate/poly-2 interface. As indicated on the SEM insert, this insufficient arsenic diffusion can be detected with an HF-nitric junction stain.

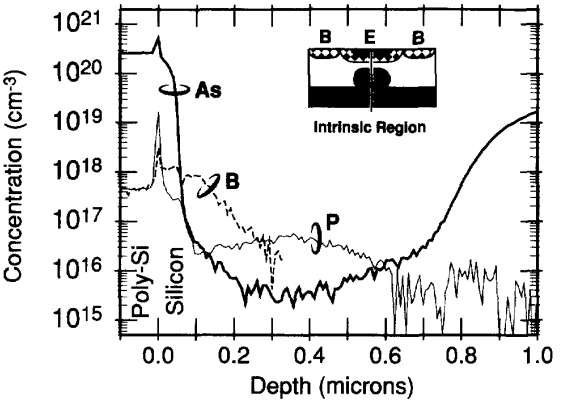

Fig. 12. SIMS profile of dopant concentration as a function of depth for the intrinsic region of a SCC BJT. Arsenic forms the diffused emitter and buried layer, boron forms the implanted base, and phosphorus forms the implanted collector.

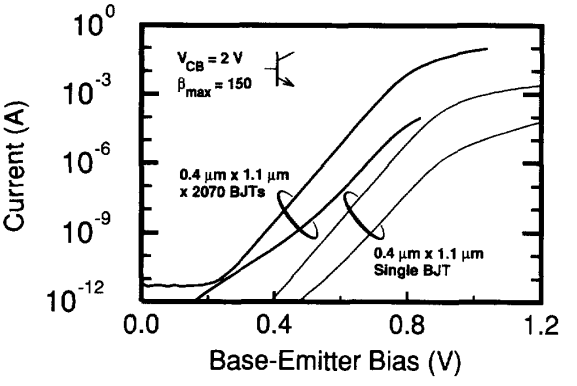

Fig. 14. Characteristic Gummel plot for the minimum-sized 0.4 μm $\times$ 1.1 μm SCC BJT. Both a discrete device and a 2070 parallel device defect array are shown.

contact resistances were extracted by forward biasing the base-collector junction of near-identical bipolar transistors, which had varying poly-substrate overlaps. The contact resistance was extracted as the slope of resistance at 1.0 V versus inverse contact area.

Although 20 keV B^{11} results in a consistently good base contact, the large extrinsic base depth then requires significant silicon trenching during the base (gate) poly-1 overetch for two reasons. First, this trenching establishes a vertical offset between the heavily doped emitter and extrinsic base regions, increasing the base-emitter breakdown voltage BV_{EBO} above 5.0 V, and leading to ideal base-current behavior. This is because the MOSFET spacer width scaled to ~1000 Å for this generation technology, which does not form a sufficiently large lateral offset between these heavily doped regions. Second, the 20 keV base poly implant tails down into the active region of the bipolar device which the trenching subsequently removes. For our process, the minimum trenching required is 0.18 μm to ensure that the base poly implant does not augment the base Gummel number set by the light, intrinsic-base implant. See Fig. 11, which shows a decrease in intrinsic base resistance (increase in Gummel number) for trench depths below 0.18 μm. The extraction of the trench depth used adjacent capacitance structures; see [13].

To ensure consistent bipolar device characteristics, a silicon trench depth of 0.24 μm was used, resulting in a calculated zero-bias R_{BX} as low as 500 Ω μm ratioed to the length of the poly cut. Thus, for a minimum-sized 0.4 μm $\times$ 1.1 μm BJT with a poly-cut of 0.7 μm $\times$ 1.4 μm, a zero-bias R_{BX} of $500/(0.7 + 1.4) = 240\Omega$ is obtained.

VIII. Emitter Plug Effect

Fig. 12 shows the SIMS profile of dopant concentration as a function of depth for the intrinsic region of a SCC BJT. The arsenic n+ buried layer and the implanted phosphorus (SCC) collector were discussed previously. The active base is implanted before spacer formation, to ensure a good link-up with the extrinsic base regions outdiffused from poly-1. As a drawback to this approach, the active base is exposed to more thermal annealing, and therefore broadens.

TABLE I
TABULATED ELECTRICAL CHARACTERISTICS OF THE 0.4 μm BY 1.1 μm SCC BJT

$W_E \times L_E$	0.4 x 1.1 μm^2	R_{BX}	240 Ω
BV_{EBO}	5.4 V	C_{BE}	5.5 fF
BV_{CBO}	19 V	C_{BC}	4.0 fF
BV_{CSO}	20 V	C_{CS}	16.3 fF
BV_{CEO}	5.0 V	C_{CS} @ 3V	9 fF
BV_{CES}	18 V	β	120
R_E	50 Ω	f_{Tmax}@1V	17 GHz
R_{BI}	10 kΩ/□	τ_{ECL}	50 ps @ 200 μA

The emitter is outdiffused from poly-2, which is previously implanted with arsenic. Similar to the extrinsic base formation, insufficient heat to drive the dopants to the substrate/poly-2 interface severly degrades the bipolar characteristics, leading to poor base current ideality ~2 and therefore low current gain and abnormally large and scattered values of BV_{EBO}. Interestingly, the emitter resistance as determined by the open collector method did not show any degradation.

As in [14], we found the most reliable indication that the arsenic was not diffusing down the poly-2 "emitter plug" was an increase of β with increasing emitter width, since widening the emitter reduces the severity of the plug's aspect ratio, reducing its total depth. In extreme cases, the resulting Gummel plots show severe degradation; see Fig. 13. This device had a tall poly-1 stack height of 4950 Å, planarized emitter poly, and an ~1050°C, 20 second RTA. The SEM insert shows that in this extreme case a short HF-nitric junction stain can detect the insufficient arsenic diffusion. Even though the accuracy of junction staining severely degrades in the presence of metalized (or polycided) wafers, the absence of arsenic dopants at the bottom of the emitter plug slows the etch rate sufficiently to highlight the emitter plug effect; see illustration arrow. In comparison, the SEM in Fig. 9, for a good bipolar device (2750 Å poly-1 stack height, ~1100°C RTA, and unplanarized poly-2) shows no such effect.

IX. SCC BJT CHARACTERIZATION

The emitter plug effects were overcome despite the thermal constraints of the core CMOS process by reducing the poly-2 plug depth both by using unplanarized poly-2 and by reducing the poly-1 stack height. Fig. 14 shows the resulting Gummel plot for the minimum-sized 0.4 μm × 1.1 μm device. Both a discrete device and a 2070 parallel device defect array are shown. The discrete device shows the excellent drive current at an applied bias of 1.2 V: 2.45 mA, corresponding to a current density of 5.6 mA/μm^2 with $\beta > 33$.

Fig. 15 shows the measured capacitances as a function of reverse bias for the collector-substrate (C_{CS}) and base-collector (C_{BC}) junctions of a 0.4 μm by 1.1 μm SCC BJT. In addition, the total substrate junction capacitance, C_R, of a discrete 2.4 μm by 1.6 μm^2 ECL resistor is shown. The

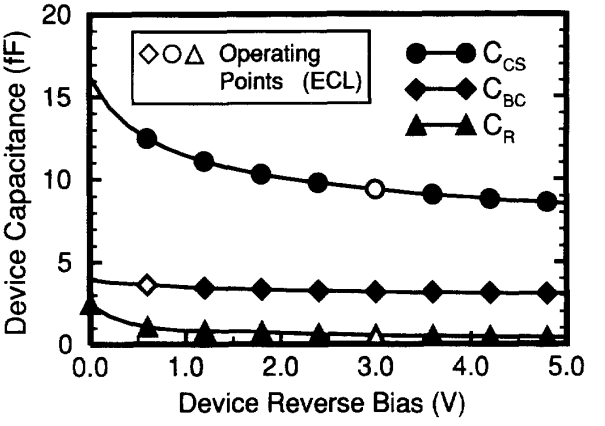

Fig. 15. Measured capacitance as a function of reverse bias for the collector-substrate (C_{CS}) and base-collector (C_{BC}) junctions of a 0.4 μm by 1.1 μm SCC BJT. In addition, the total substrate junction capacitance, C_R, of a discrete 2.4 μm by 1.6 μm^2 ECL resistor is shown.

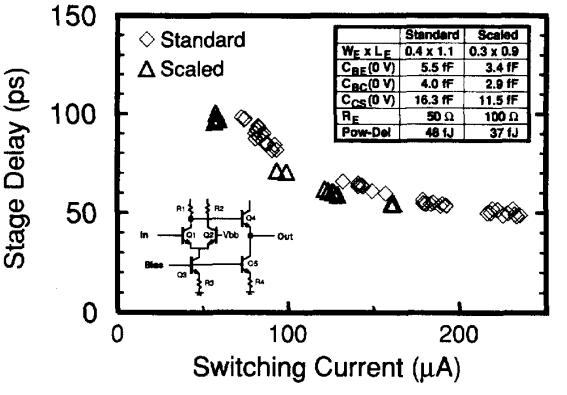

Fig. 16. Measured stage delay versus switching current for a conventional single-ended ECL gate with $\Delta V = 0.5$ V. Some of the key parasitics for both the standard and scaled SCC BJT are indicated. The listed power-delay product is at the minimum switching current.

ECL operating points are also indicated, since the zero-bias value of C_{CS} can be misleading in comparing trench isolated devices, where C_{CS} does not decrease much with reverse bias, to junction isolated devices, where C_{CS} does decrease with reverse bias. Note that this decrease is not as dramatic as shown in Fig. 7, due to the diffusion of the collector and p well regions to form nonabrupt junctions, and the parallel capacitance contribution of the area component. A summary of key parameters is given in Table I.

X. DEVICE SCALABILITY

The alignment tolerances of the SCC BJT structure are relatively relaxed, since this transistor is used in the periphery only. To evaluate the scalability of the transistor, the SCC BJT was shrunk to match the alignment tolerances of the bit cell. This has the drawback of increasing a number of the parasitic series resistances, but has the advantage of reducing the parasitic junction capacitances. The table insert of Fig. 16 shows this capacitance improvement, with a ~30% reduction for the

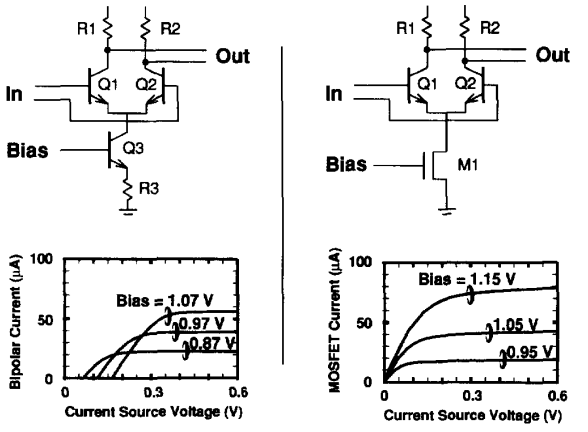

Fig. 17. (a) Current-Mode Logic (CML) gate with a conventional bipolar current source, versus (b) a n-MOS current source. The accompanying simulations show that use of an n-MOS transistor reduces the voltage drop across the current source (I_S) for these CML gates. The resistors are identical, with a constant 200 mV voltage drop across R3 (400 mV differential signal).

three primary components. These parasitics are comparable to other high-performance bipolar-only technologies.

XI. ECL Circuit Performance

Fig. 16 also shows the measured stage delay versus switching current for a conventional single-ended ECL gate with $\Delta V = 0.5$ V. The scaled SCC BJT has a 23% lower power-delay product at low currents, owing to its lower parasitic capacitances, but this advantage diminishes at higher current levels. The standard device obtains sub-50 ps delays at 225 μA switching current. Although the standard device was also laid out with an emitter area of 0.6 μm × 1.1 μm, the ECL performance was virtually identical to the 0.4 μm × 1.1 μm device. This is because the parasitic capacitances of such small devices are perimeter dominated.

XII. Modified CML Logic Gate

Since even aggressive scaling of the SCC BJT showed only a 23% improvement in power-delay product, substantial improvements in this figure of merit are possible only through a substantial structural change, or a modification of the logic gate. Fig. 17(a) shows one such gate, the Current-Mode Logic (CML) gate with a conventional bipolar current source. The current of this gate is lower than that of Fig. 16 because a separate emitter follower stage is not required, and the switching voltage (and therefore current) can be reliably reduced from 500 mV to 200 mV because the output is differential. Furthermore, since this gate does not stack bipolar diode drops, the minimum operating voltage is lower, allowing additional power reduction. The operating voltage can be further reduced by using a readily available n-MOS current source; see Fig. 17(b). As shown by the accompanying simulations, the n-MOS current source operates down to voltages 0.2 to 0.3 V lower than the conventional bipolar source. It is important to note that this is a nearly "fair" comparison despite the presence of resistor R3. E.g., for both current sources operating at 40μA, ±100 mV of noise at the bias node results in a current fluctuation of ~ ±50%. Removal of R3 would result in ±100 mV of noise creating over three orders of magnitude variation in the bipolar current source.

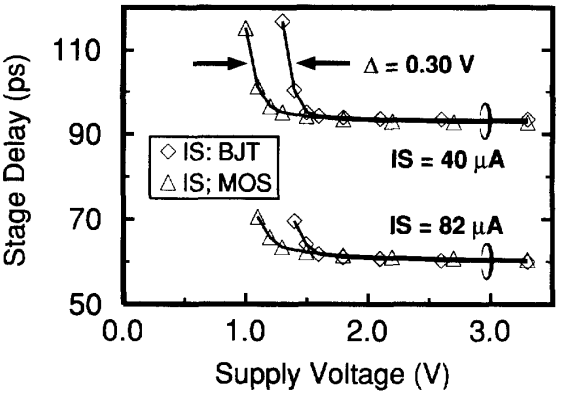

Fig. 18. Measured CML gate delay versus supply voltage for two different load resistances. The differential signal swing is 400 mV. Use of a MOS current source (see Fig. 17) increases the "voltage headroom" by 0.3 V.

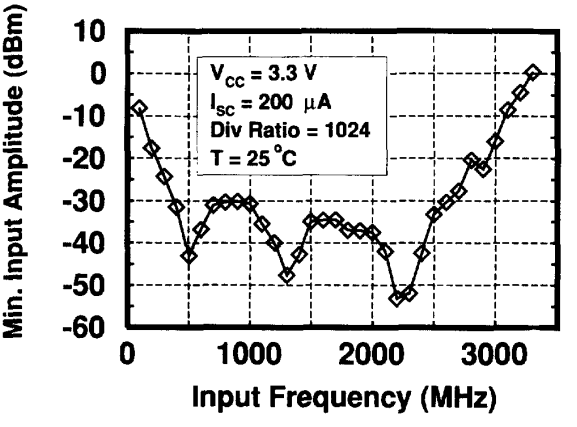

Fig. 19. Input signal sensitivity of the ÷ 4/5 prescaler, showing a maximum input frequency of 3.3 GHz.

XIII. Measured CML Performance

The CML performance reported here is for the scaled BJT. Even for this scaled device the layout area is larger than that for a MOSFET, so that the modified CML gate with the smaller MOSFET and no resistor R3 represents a significant layout area saving. As seen in Fig. 18, this modification extends by up to 0.3 V the minimum operating voltage of the gate, allowing operation down to 1.0 V. Because standard CML logic usually involves bipolar stacking, this additional "voltage headroom" is already of importance at a 3.3 V supply.

At a supply voltage of 1.1 V, and at 40 μA switching current, the minimum power-delay product of the CML gate is a silicon-substrate bipolar record 4.5 fJ. This extremely low value is an order of magnitude lower than the ECL value we

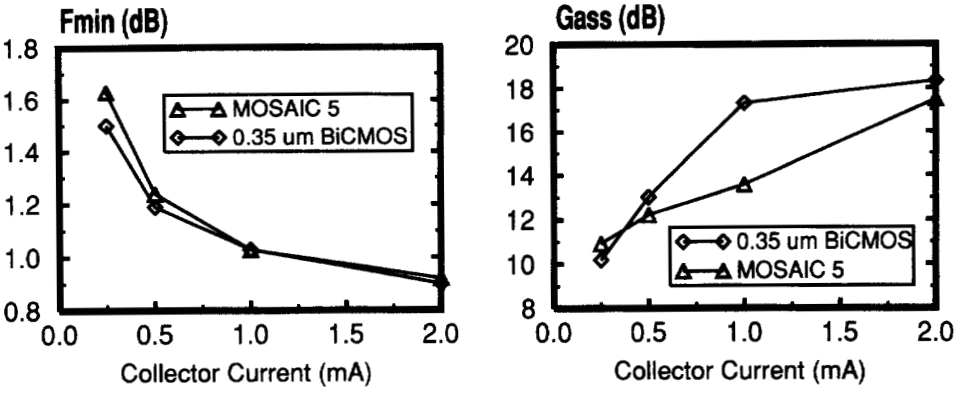

Fig. 20. Minimum noise figure, $F_{\min}$, and associated gain, G_{ass}, for packaged RF bipolar devices with $L = 9 \times 19.2\mu$m. As a comparison, data for the bipolar-only process MOSAIC 5 is presented. $F = 900MHz, V_{\text{CE}} = 1.0$V.

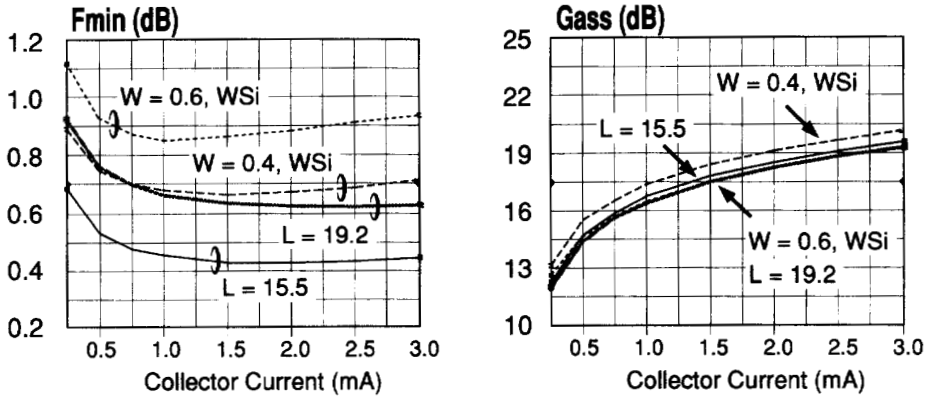

Fig. 21. De-embedded minimum noise figure, $F_{\min}$, and associated gain, G_{ass} at $F = 900$ MHz and $V_{\text{CE}} = 1.0$ V for 4 different bipolar topologies with approximately the same drawn emitter area. Strapping the base with only WSi rather than metal-1 does not increase $F_{\min}$, but increases the gain by 1.5 dB due to the reduction in base area and therefore C_{BC} ($W = 0.4$, WSi). Increasing the emitter width increases the noise figure due to an increase R_B ($W = 0.6$, WSi). The RF device with shorter emitter fingers also has more metal strapping, which may reduce its noise figure ($L = 15.5$).

last reported [15], and compares to a CML value of 8.6 fJ at a supply of 1.8 V for a 0.2 μm $\times$ 1.6 μm BJT in an SOI-based, deep-trench bipolar-only technology [16].

XIV. RF Results

A common benchmark circuit for RF applications is the dual modulus $\div$ 4/5 prescaler. For this purpose, the 0.4 μm $\times$ 1.1 μm SCC BJT was used, and a conventional bipolar design was implemented with a switching current of 200 μA and a differential signal swing of 600 mV. At the output of the prescaler, a chain of eight divide-by-two stages divide the output signal frequency by 256 to simplify the characterization. In addition, input and output buffers provided signal conditioning. At a supply voltage of 3.3 V and at room temperature, a maximum input frequency of 3.3 GHz was achieved. The input signal sensitivity of the prescaler is shown in Fig. 19; an input signal of -15 dBm results in a frequency operating range from 170 MHz to 3 GHz. When the supply voltage is reduced to 2.7 V, the performance of the prescaler, although acceptable, is degraded; at 2.5 GHz, the minimum input signal level increases from -33 to -25 dBm.

The RF device of Fig. 20 is substantially larger than minimum and has nine 19.2 μm-long interdigitated emitter fingers, resulting in a calculated $R_B \approx 2.8\Omega$. Under the active bias of $V_{\text{CE}} = 1.0$ V and 0.5 mA, the small-signal equivalent circuit extracted using s-parameter measurements resulted in $R_B = 3.8\Omega$. The total base resistance, R_B, the minimum noise figure, $F_{\min}$, and associated gain, G_{ass}, were measured including packaging. As a comparison, data for the bipolar-only process MOSAIC 5 [3] is also presented, showing equivalent performance. All measurements presented here were taken at $V_{\text{CE}} = 1.0$ V and a frequency of 900 MHz.

Fig. 21 shows the de-embedded minimum noise figure, $F_{\min}$, and associated gain, G_{ass} at $F = 900$ MHz and $V_{\text{CE}} = 1.0$ V for 4 different bipolar topologies with nearly the same drawn emitter area ~ 60 μm^2. The $W = 0.4$ μm device of the previous figure is labelled with its emitter length of $L = 19.2$ μm. By using more but shorter ($L = 15.5$ μm) emitter fingers, the noise figure can be further reduced. This results

in a 0.54 dB noise figure at 900 MHz and 0.5 mA with an associated gain of 14.7 dB. Since the base poly is strapped by WSi, the parallel metal-1 strapping of the base which is usually employed to drive down R_B for low-noise RF performance is not required when short (6.6 μm) emitter fingers are used. This increases the gain by $\sim$ 1.5 dB due to the reduction in base area and therefore C_{BC} (W = 0.4, WSi).

XV. Conclusion

We presented the process development and device characterization of the Selectively Compensated Collector (SCC) BJT specifically designed for high-density deep-submicrometer BiCMOS SRAM technologies. This double-poly BJT takes advantage of the self-aligned polysilicon layers of the SRAM bit cell to obtain high performance without adding excessive process complexity. Furthermore, although an NPN device, the SCC BJT is formed in a lightly doped p-well in which the collector is formed with a single 370 keV phosphorus implant to minimize parasitic junction capacitances. The suitability of this bipolar structure outside of its original FSRAM intent is proven with its potential for bipolar logic and mixed-mode RF applications. ECL delays of 50 ps at 200 μA and a CML power-delay product of 4.5 fJ at 1.1 V supply were obtained. A 900 MHz noise figure as low as 0.54 dB at 0.5 mA with an associated gain of 14.7 dB was demonstrated as well as a dual modulus $\div$4/5 prescaler operating up to 3.3 GHz for a switch current of 200 μA.

Acknowledgment

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References

[1] S. Konaka, E. Yamamoto, K. Sakuma, Y. Amemiya, and T. Sakai, "A 20-ps Si bipolar IC using advanced super self-aligned process technology with collector ion implantation," *IEEE Trans. Electron Devices*, vol. 36, no. 7, pp. 1370–1375, 1989.

[2] M. Sugiyama, H. Takemura, C. Ogawa, T. Tashiro, T. Morikawa, and M. Nakamae, "A 40 GHz f_T Si bipolar transistor LSI technology," in *IEDM Tech. Dig.*, 1989, pp. 221–224.

[3] V. de la Torre, J. Foerstner, B. Lojek, K. Sakamoto, S. L. Sundaram, N. Tracht, B. Vasquez, and P. Zdebel, "MOSAIC V—A very high performance bipolar technology," in *Proc. IEEE Bipolar Circuits and Technol. Meeting*,1991, pp. 21–24.

[4] J. Warnock, J. D. Cressler, K. A. Jenkins, T.-C. Chen, J. Y.-C. Sun, and D. D. Tang, "50-GHz self-aligned silicon bipolar transistors with ion-implanted base profiles," *IEEE Electron Device Lett.*, vol. 11, no. 10, pp. 475–477, 1990.

[5] S. Nakamura, T. Toyofuku, M. Sueda, K. Hasegawa, I. Kato, and T. Takada, "Bipolar technology for a 0.5-micron-wide base transistor with an ECL gate delay of 21.5 picoseconds," in *IEDM Tech. Dig.*, 1992, pp. 445–448.

[6] G. L. Patton, J. H. Comfort, B. S. Meyerson, E. F. Crabbe, G. J. Scilla, E. De Fresart, J. M. C. Stork, J. Y.-C. Sun, D. L. Harame, and J. N. Burghartz, "75-GHz f_T SiGe-base heterojunction bipolar transistors," *IEEE Electron Device Lett.*, vol. 11, no. 4, pp. 171–173, 1990.

[7] F. Sato, T. Hashimoto, T. Tatsumi, H. Kitahata, and T. Tashiro, "Sub-20psec ECL circuits with 50 GHz fmax self-aligned SiGe HBTs," in *IEDM Tech. Dig.*, 1992, pp. 397–400.

[8] M. R. Pinto, C. S. Rafferty, and R. W. Dutton, *PISCES II: Poisson and Continuity Equation Solver*, Stanford University, 1984.

[9] R. C. Taft, J. D. Hayden, and C. D. Gunderson, "Optimization of two-dimensional collector doping profiles for submicron BiCMOS technologies," in *IEDM Tech. Dig.*, 1991, pp. 869–872.

[10] J. A. Bruchez and P. Pollok, "The philosophy of a simple collector diffusion isolation bipolar process," *Solid State Technology*, pp. 93–97.

[11] J. D. Hayden *et al.*, "A high-performance quadruple well, quadruple poly BiCMOS process for fast 16 Mb SRAMs," in *IEDM Tech. Dig.*, 1992, pp. 819–822.

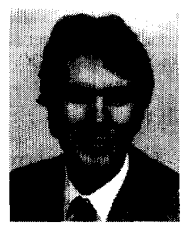
[12] V. Probst, H. Schaber, A. Mitwalsky, H. Kabza, L. V. den jove, and K. Maex, "WSi_2 and $CoSi_2$ as diffusion sources for shallow-junction formation in silicon," *J. Appl. Phys.*, vol. 70, no. 2, pp. 708–719, 1991.

[13] R. C. Taft and S. Noell, "Device structure characterization using the comparative CV technique," *J. Vac. Sci. Technol.*, vol. B-12, no. 1, pp. 332–335, 1994.

[14] J. N. Burghartz, J. Y.-C. Sun, C. L. Stanis, S. R. Mader, and J. D. Warnock, "Identification of perimeter depletion and emitter plug effects in deep-submicrometer, shallow-junction polysilicon emitter bipolar transistors," *IEEE Trans. Electron Devices*, vol. 39, no. 6, pp. 1477–1489, 1992.

[15] R. C. Taft, J. D. Hayden, D. J. Denning, and H. C. Kirsch, "A high-performance low-complexity bipolar technology using selective collector compensation," in *IEDM Tech. Dig.*, 1992, pp. 405–408.

[16] E. Bertagnolli, H. Klose, R. Mahnkopf, A. Felder, M. Kerber, M. Stolz, G. Schutte, H.-M. Rein, and R. Köpl, "An SOI-based high performance self-aligned bipolar technology featuring 20 ps gate-delay and a 8.6 fJ power-delay product," in *Symp. VLSI Technol. Dig. Tech. Papers*, 1993.



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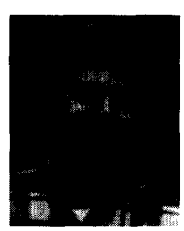
In October 1990, he joined the APRDL division of Motorola and designed the Selectively Compensated Collector (SCC) bipolar transistor for Motorola's 0.35 μm BiCMOS SRAM technology. His responsibilities broadened to include the 0.35 μm BiCMOS pilot baseline and to assist the SRAM memory design group. In August 1994, he joined East Coast Labs, Salem, NH, a start-up fabless semiconductor company.



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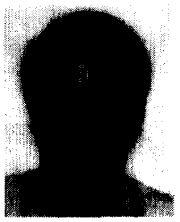

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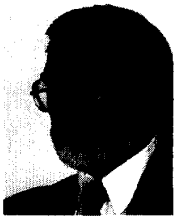

H. C. Kirsch received the B.S. degree from Case Tech in 1966 and the Ph.D. degree in applied physics from Stanford University, Stanford, CA, in 1972.

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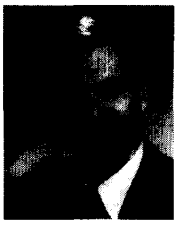

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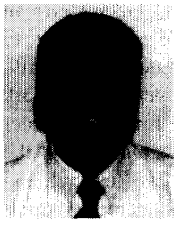

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He joined Texas Instruments Central Research Labs in 1985. There he conducted research on millimeter wave devices and circuits. Some of the technologies he worked on include GaAs MESFET's, HEMT's, IMPATT's, GUNN's, and HBT's. He was also part of the original team that kicked off the development power GaAs HBT's. He joined Avantek (now a subsidiary of HP) in 1988. There he developed several hybrid and monolithic millimeter wave circuits and subsystems using GaAs MESFET's and PHEMT's. He was in charge of several subsystems projects and government R&D programs. In 1990 he joined Motorola Semiconductor Products Sector as a Manager within the sector technology organization. He was part of the management team that started the GaAs effort in Motorola where he was in charge of design and applications. During this time period, he demonstrated designs for CT2, DECT, and cellular markets. He then went on to work on silicon RF technologies. His group characterized, modeled, and enhanced Motorola's RF technologies which included BJT, LDMOS, and BiCMOS technologies. Later on he fathered the concept of RF-LDMOS IC's for power applications and was instrumental in the development of this technology. In 1995, he joined Advanced Micro Devices, Sunnyvale, CA, as the Radio Development Manager.