Thermally Robust $TiSi_2$ on Heavily Doped Polycrystalline Silicon over Severe Topography

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ABSTRACT

Using $TiSi_2$ to strap polysilicon over severe topography is hampered by the non-conformality of sputter deposited titanium (Ti) films. Thinning of the Ti translates into regions with thin silicide which degrade drastically when subject to 900°C anneals. Etching back a thick polysilicon film to the desired thickness planarizes the surface for Ti deposition and eliminates the influence of underlying topography. The fabrication process outlined provides a final $TiSi_2$ sheet resistance ~ 2 Ω/□, after a 900°C anneal in O_2.

INTRODUCTION

The use of low resistivity silicided polysilicon (polycide) layers has emerged as a necessity when ULSI fabrication technologies realize SRAMs of 4Mbit size and larger. Tungsten silicide (WSi_2) and titanium silicide ($TiSi_2$) appear favored amongst refractory metal silicides to reduce the resistivity of polysilicon when used as an interconnect [1-4]. The inherent conformality of chemical vapor deposition (CVD) favors WSi_2 when the polycide needs to travel over underlying topography. The high (50-70 μΩ-cm) resistivity of WSi_2 relative to $TiSi_2$ (13-16 μΩ-cm) is, however, a drawback in fabricating low resistance interconnects. Further, the self-aligning feature of forming $TiSi_2$ via interfacial reaction of a deposited titanium (Ti) film, circumvents the need to etch a silicide/polysilicon stack.

In order to achieve higher device densities, ULSI technologies tend to require multiple levels of polysilicon/polycide and metal. The severity of the topography encountered by a polycide layer depends on when it is used in the fabrication sequence. The first polysilicon level usually constructs MOSFET gate electrodes and extrinsic base contacts for fully-self-aligned (FSA) bipolar transistors, and thus only passes over field oxide topography. The topography under all subsequent levels of polysilicon can be severe and will vary depending on the use of intermediate planarization. Due to this underlying topography the silicide thickness in a $TiSi_2$/polysilicon bilayer is not uniform, since the deposited Ti films have imperfect conformality. The sensitivity of $TiSi_2$ to thermal degradation depends strongly on film thickness [5,6]. Silicide thinning, therefore, poses a possible limitation to using $TiSi_2$ when the polycide has to experience high temperature anneals. This paper discusses forming $TiSi_2$ on heavily arsenic (As) doped polysilicon which forms bipolar transistor emitters, self-aligned contacts to MOSFET source-drains and provides an interconnect layer in BiCMOS technologies at 0.5 μm and below, and how the above mentioned limitation may be overcome.

THE PROBLEM

The polysilicon used here was 2500Å thick and doped via implantation (As, 90 keV, 8E15 cm^{-2}) followed by rapid

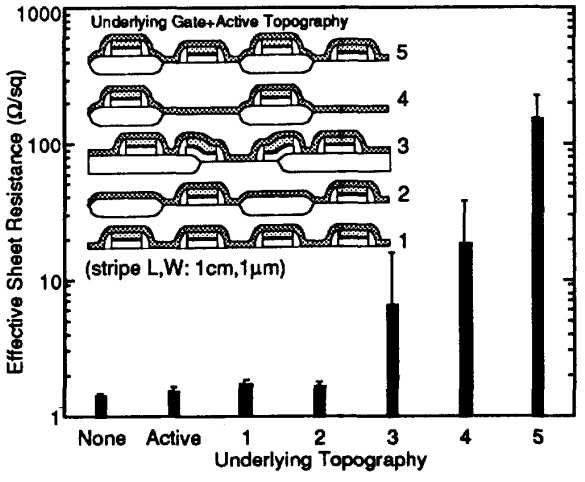

Fig. 1 Effective R_{sh} of a polycide stripe after a 900°C, O_2, 15 min, anneal as a function of underlying topography.

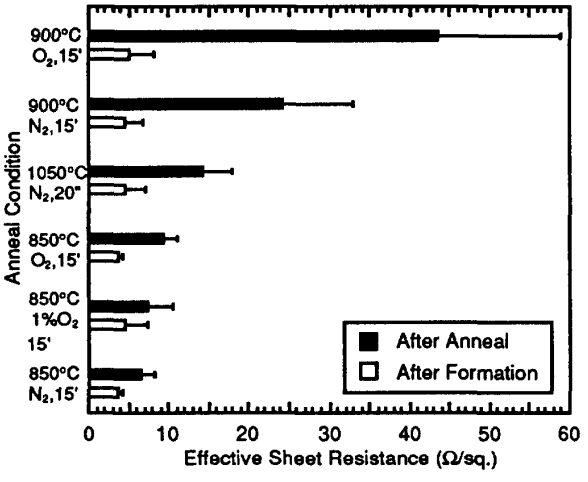

Fig. 2 Impact of anneal ambient and temperature on the conductivity of a polysilicon stripe silicided using 400Å of Ti.

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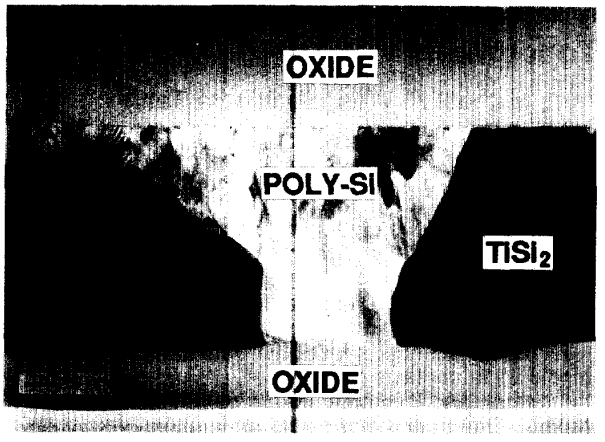


Fig. 3 TEM cross section of a silicided polysilicon sheet film after a 900°C, O_2, 15 min anneal. (Ti = 400Å)

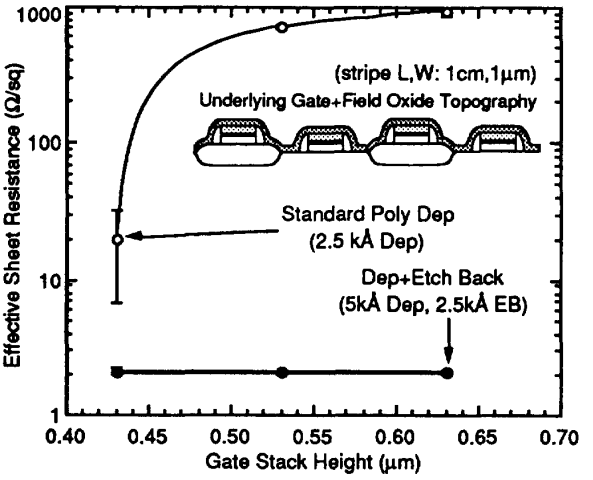


Fig. 4 Effective R_{sh} of a polycide stripe after a 900°C, O_2, 15 min anneal as a function of gate electrode height.

thermal annealing (RTA). The silicide formation process consisted of an in-situ Ar back-sputter clean, 600Å of sputter deposited Ti, a silicon implant to mix the titanium-polysilicon interface, a 700°C RTA in a nitrogen ambient, a Ti/TiN wet etch in a $NH_4OH:H_2O_2:H_2O$ solution and a second RTA at 850°C also in nitrogen. During backend thermal treatment, the polycide was covered with tetraethylorthosilicate (TEOS) oxide deposited by low pressure chemical vapor deposition (LPCVD).

The effective sheet resistance of a 1 μm wide, 1 cm long, $TiSi_2$/polysilicon stripe after a 900°C, 15 min anneal in oxygen is plotted in Fig. 1, for various underlying topographies. As the data indicates the disintegration of the bilayer and associated increase in overall resistance is clearly dependent on underlying topography specifics. While no significant degradation occurs when the polycide passes over only gate electrodes, the resistance increases dramatically when various combinations of gate electrode and field oxide patterns are present. Besides film thickness, the resistivity increase due to thermal disintegration of $TiSi_2$ is also dependent on the anneal ambient and temperature as seen in Fig. 2. Agreeing with previous results [5] oxygen ambients are found to degrade the silicide more than those containing nitrogen. This work has explored forming a polycide capable of withstanding a 900°C anneal in oxygen. The degradation of $TiSi_2$ when subjected to high temperatures occurs

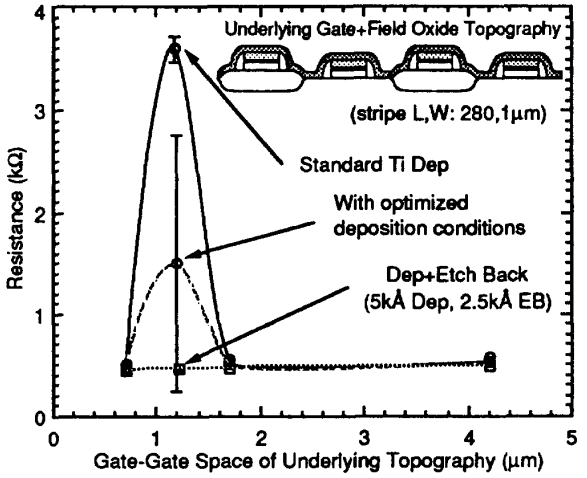


Fig. 5 The resistance of a $TiSi_2$/polysilicon stripe after a 900°C, O_2, 15 min anneal as a function of gate electrode space.

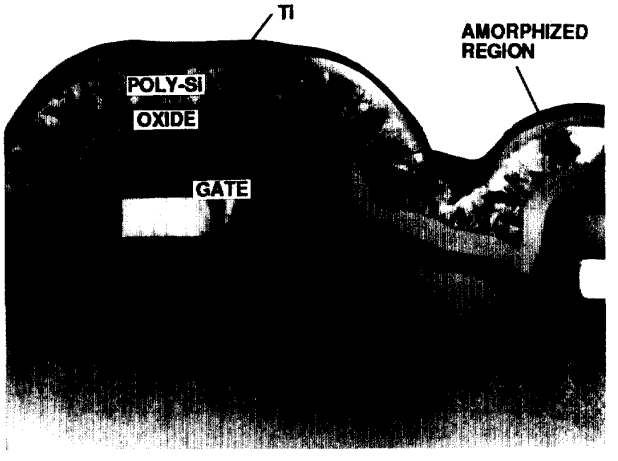


Fig. 6 TEM cross section of the polysilicon layer after titanium deposition and the silicon interface mixing implant.

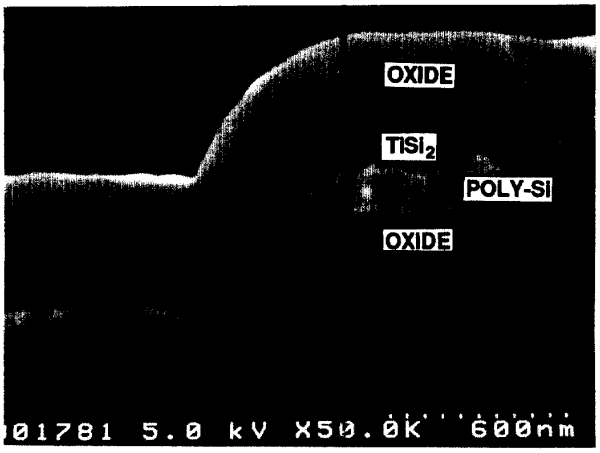


Fig. 7 SEM cross section of the silicided polysilicon layer illustrating silicide thinning at a gate electrode step.

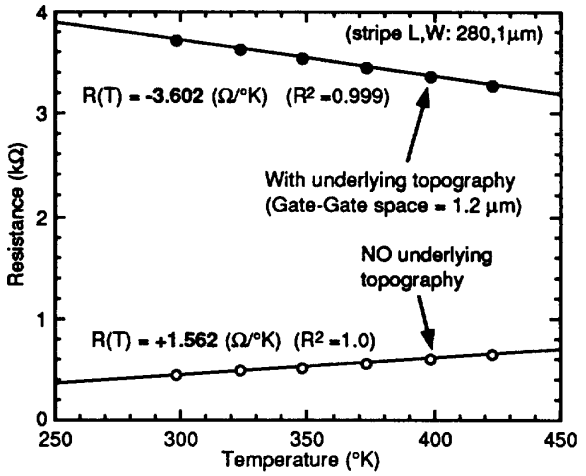


Fig. 8 The temperature dependence of polycide resistance after a 900°C, O_2, 15' anneal with and without topography.

by agglomeration [5,6] as seen in Fig. 3. The silicide shown in this TEM was formed using 400Å of Ti on polysilicon implanted with an As dose of 3E15 (cm^{-2}).

As seen in Fig. 4, as the height of the gate electrode increases so does the effective polycide sheet resistance of a narrow stripe. For taller gate stacks, thinning of the $TiSi_2$ is aggravated which leads to worse degradation during the 900°C anneal. The resistance of a polycide stripe as a function of the gate electrode pitch is plotted in Fig. 5. The data indicates that the thermal degradation related resistivity increase of a $TiSi_2$/polysilicon bilayer is dictated by the underlying gate electrode pitch besides sheer step height. Thus, in addition to the verticality of the polysilicon surface the titanium film can also be thinned by creating a narrow crevice, the bottom of which the sputtered metal cannot reach.

Thinning of the Ti film and the region amorphized by the Si implant, can be clearly seen in Fig. 6 which shows the polysilicon layer after Ti deposition and the mixing implant, obtained using cross section transmission electron microscopy (XTEM). The silicide thickness variation in the polycide caused by the thinner titanium in the more vertical regions, is seen in Fig. 7. These sections of thin $TiSi_2$ degrade via agglomeration as shown earlier, and due to the ~$x10^3$ higher diffusivity of arsenic in $TiSi_2$ relative to Si [7], disconnected islands of polysilicon are formed which

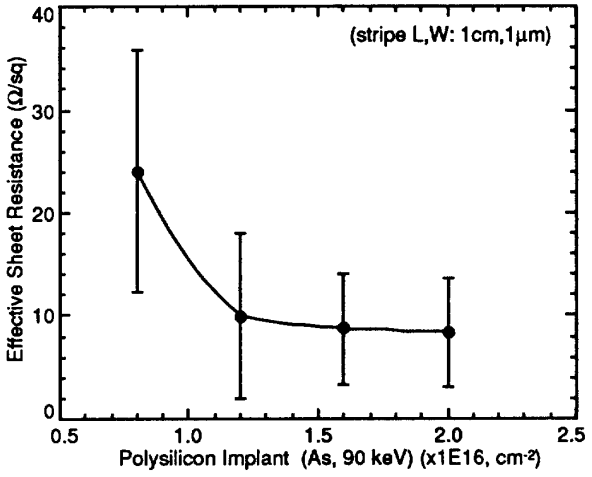


Fig. 9 The dependence of polycide resistivity after a 900°C, O_2, 15 min anneal on the polysilicon implant flux.

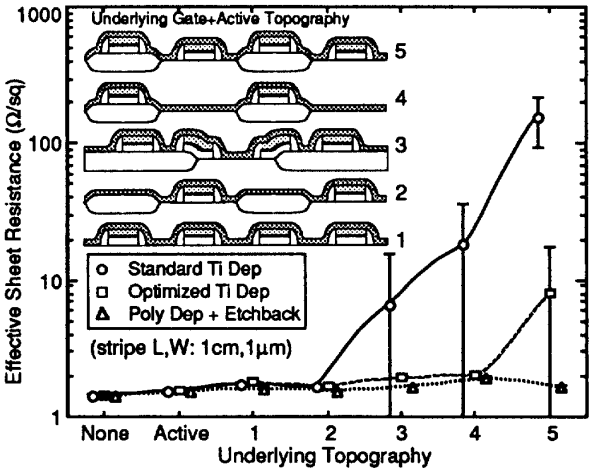
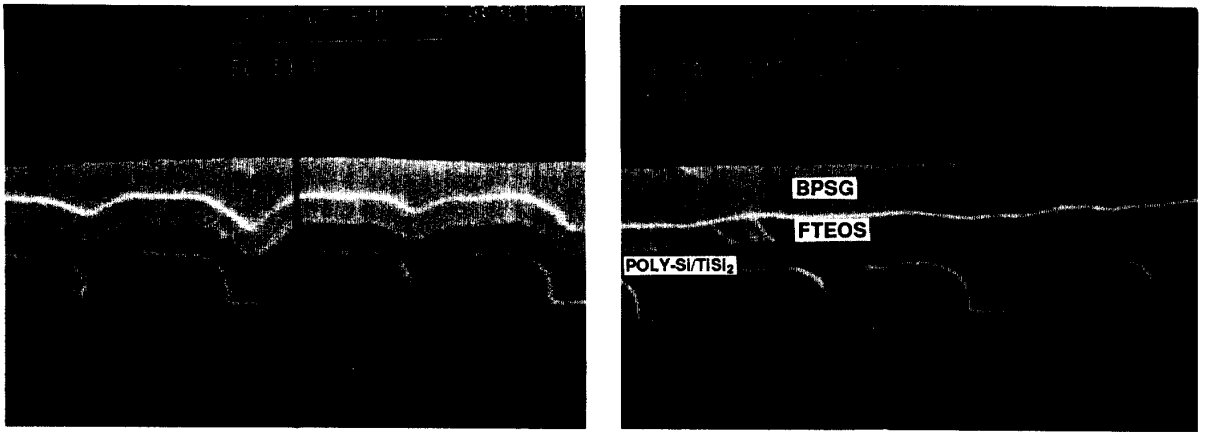


Fig. 10 Effective R_{sh} of a polycide stripe after a 900°C, O_2, 15 min anneal as a function of underlying topography.



(a) (b)

Fig. 11 SEM cross sections of a silicided polysilicon stripe after a 900°C, O_2, 15 min anneal. In the two photographs, the polysilicon was formed by (a) a single 2500Å deposition, (b) etching a 5000Å film down to 2500Å.

which are depleted of dopant. These lightly doped polysilicon regions dominate the net resistance of the polycide. Seconding this postulation is the transition of the temperature coefficient (R_{TT}) of the silicided polysilicon resistivity when underlying topography is introduced, which is shown in Fig. 8. On a flat surface $TiSi_2$/polysilicon resistivity has a positive value of R_{TT}, indicating metallic carrier conduction since nearly all the current flows in the silicide. When the polycide layer passes over topography, however, the R_{TT} becomes negative indicating carrier transport similar to that of a semiconductor, since the overall resistance is now dominated by polysilicon regions. Arsenic segregation into the silicide during the high temperature anneal can also be seen in Fig. 9. The resistivity of a narrow $TiSi_2$/polysilicon stripe after a 900°C anneal in oxygen is shown to decrease when more arsenic is initially present in the polysilicon.

A SOLUTION

Thus the main obstacle to using $TiSi_2$ to strap polysilicon over severe topography, when high temperature backend heat cycles are needed, is the non-conformality of the Ti film. Increasing the Ti thickness does result in thicker silicides which have superior thermally stability. However, the maximum usable Ti thickness is determined by the fraction of the polysilicon consumed in the silicidation reaction. Optimizing the sputter deposition process does reduce the sensitivity of $TiSi_2$/polysilicon thermal degradation to underlying topography as seen in Fig's 5 and 10, but fails to eliminate it.

Since the cause of this problem is the poor step coverage of sputter deposited films, one way to overcome it is to eliminate or reduce the acuteness of the steps. This can be achieved by planarizing either the polysilicon surface or the surface beneath it. Etching back a thick polysilicon layer to the desired thickness achieves a smoother surface than if a single deposition was used, as seen in Fig. 11. The data in Fig's 4, 5 and 10 show that this technique does successfully eliminate the sensitivity of $TiSi_2$/polysilicon thermal degradation to underlying topography. When the polycide forms emitter contacts in FSA bipolar devices, the etch back technique fills up the spaces between adjoining gate electrodes and thus moves the silicide further away from the polysilicon/monosilicon interface. This allows for thicker silicides to be formed on the emitter polysilicon without impacting bipolar performance.

CONCLUSIONS

The thermal degradation of $TiSi_2$ on polysilicon over severe topography occurs due to non-conformal Ti films. Thinning of sputter deposited titanium translates into thinner silicides which degrade drastically when subject to 900°C anneals. Etching back a thick polysilicon film to the desired thickness planarizes the surface for Ti deposition and eliminates the influence of underlying topography. The fabrication process outlined provides a final $TiSi_2$ sheet resistance ~ 2 Ω/□, after a 900°C anneal in O_2, providing an useful alternative to CVD WSi_2 as a lower resistance interconnect for a fixed polycide thickness.

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