A High Density 0.10μm CMOS Technology Using Low K Dielectric and Copper Interconnect

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ABSTRACT

In this work components of the next generation 0.10 μm CMOS technology are presented. They form the core of a platform encompassing logic, non volatile memory, and analog blocks. High performance bulk devices use 18 Å gate oxide (24 Å inversion Tox) while low power devices use 25 Å gate oxide (31 Å inversion Tox) for reduced gate leakage. Gate lengths range from 65 nm for the high performance devices to 90nm for the low power devices. Both 3.3V and 2.5V I/Os are supported using 70 Å and 50 Å oxide devices. The backend employs low-k (k ~ 3) dielectric with multiple levels of Cu metallization. The high density 6T SRAM cell size is 1.33 μm^2.

Table 1 Layout Rules for 0.10 μm CMOS Technology

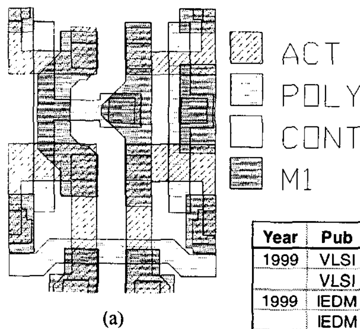
Layer	0.13 μm	0.10 μm	Shrink
Active Line/Space	0.18/0.18	0.11/0.14	31%
Poly Line/Space	0.15/0.21	0.10/0.14	33%
Contact Size/Space	0.18/0.18	0.12/0.14	28%
Contact Space to Poly	0.105	0.08	24%
Metal 1 Line/Space	0.18/0.18	0.12/0.12	33%
Metal 2-8 Line/Space	0.21/0.21	0.14/0.14	33%
Via Size/Space	0.21/0.21	0.13/0.15	33%

(a) (b)

Fig. 1 Top view SEMs of SRAM isolation pattern for (a) no corrections applied, (b) corrections applied.

PROCESS INTEGRATION

Key design rules are shown in Table 1 along with a comparison to the previous 0.13 μm process node [1]. Overall, about a 30% shrink is achieved. These rules enable a 6T SRAM cell with area of 1.33 μm^2 to be realized. Fig. 2 (a) shows the cell layout through metal 1 while Fig. 2 (b) is a list of other recently published 6T cells. In order to realize these rules, 193 nm photolithography is employed along with extensive optical proximity correction (OPC) at all critical levels. As an example of this, Fig. 1 shows the SRAM bitcell isolation pattern with and without corrections applied.

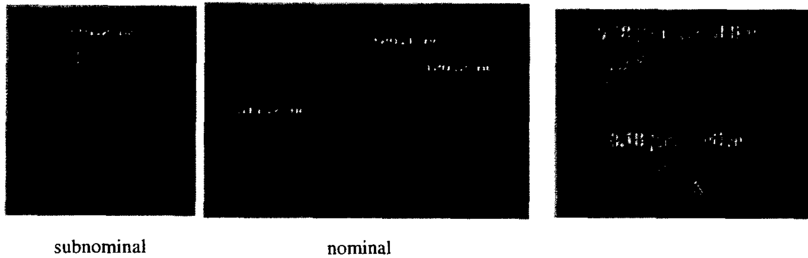


(a)

Year	Pub	Source	6T cell (um^2)
1999	VLSI	TSMC	4.4
	VLSI	IBM	3.84
1999	IEDM	NEC	3.99
	IEDM	Infineon	3.68
2000	VLSI	TSMC	3.42
	VLSI	Toshiba	2.5
	VLSI	IBM	2.16
	VLSI	Motorola	2.74
	VLSI	IBM	2.48
2000	IEDM	Motorola	2.48
	IEDM	Intel	2.09
	IEDM	TSMC	2.43
	IEDM	Sony	2.2
2001	VLSI	Hitachi	3.1
	VLSI	Infineon	2.28
	VLSI	LSI Logic	1.87
	VLSI	Toshiba	1.25
		this work	1.33

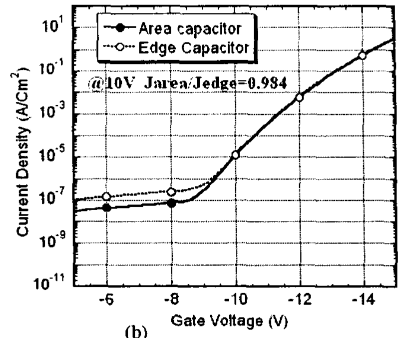
(b)

Fig. 2 (a) 1.33 μm^2 bitcell layout (b) recent reported SRAM cell sizes



subnominal nominal

Fig. 3 SEMs showing void free oxide fill of subnominal and nominal isolation trenches.



(a) (b)

Fig. 5 (a) NVM bitcell (b) tunnel oxide IV

Table 2 0.10μm Process Features

• CMOS Platform (Logic, SRAM, NVM, RF) • Shallow Trench • DGO/TGO Option • 193 nm Lithography (Active, Gate, Contact, M1) • Co-Salicide • Dual Inlaid Integration • Low K dielectric film • Low K Cu passivation

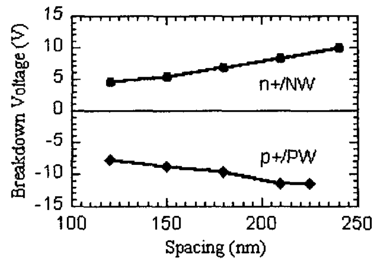


Fig. 4 Inter-well Isolation (5nA/μm BV criterion)

Key process features are listed in Table 2. In order to accommodate wireless RF applications, p- substrates are supported in addition to p- epi on p+ substrates to reduce the inductor losses. The integration starts with shallow trench isolation and a 3.5 KÅ trench depth. A high density plasma oxide fill process is used which is capable of void free fill down to below 0.12 μm wide trenches (see Fig. 3). The interwell electrical isolation is shown in Fig. 4 which illustrates low leakage down to 0.12 μm diffusion to well space.

Fig. 6 1.33 μm^2 SRAM cell post gate etch

In keeping with system-on-chip (SoC) technology requirements, the 0.10 μm technology supports an embedded NVM module. NVM cell sizes below 0.20 μm^2 are achievable without adding excessively complex processing; Figure 5 (a) shows a 0.19 μm^2 cell, and cells as small as 0.16 μm^2 are in development. Processes for isolation, gate, and metallization are developed to be NVM compatible from the beginning. For example, particular attention is paid to trench corner rounding to suppress edge tunneling currents. Fig 5(b) shows the tunnel oxide IV characteristics that exhibit no edge enhancement as desirable for reliable floating gate cell operation.

After the wells are implanted, I/O gate oxide is grown and patterned followed by an optional intermediate gate oxide and then the core gate oxide. Polysilicon gate layer is deposited and patterned with 193nm lithography. An inline SEM picture of the SRAM bitcell is shown in Fig. 6 post gate etch. Shallow extensions and conventional nitride spacers are used to control the extent of the source/drain implants. Cobalt silicide on active and poly regions is employed to reduce contact resistance and tungsten plugs connect up to a single inlaid Cu metal 1. Fig. 7 shows a cross section of the SRAM bitcell through the bitline contacts.

Fig. 7 SRAM cell post M2 Cu polish

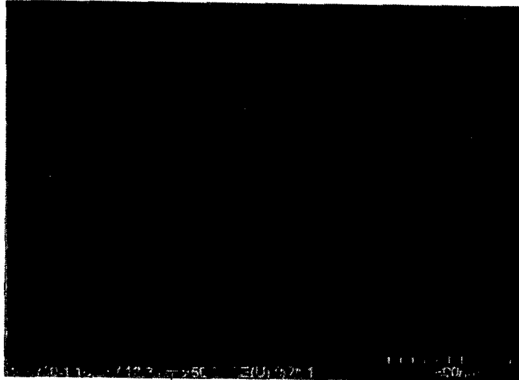


Fig. 8 Deprocessed bitcell view showing W plugs and poly with spacers

A top down SEM of the deprocessed bitcell is shown in Fig. 8. After metal 1, a dual inlaid copper integration is used to process the subsequent metal and via levels. To reduce the backend wire capacitance, a low-k dielectric film is used for both the dielectric and barrier layer.

DEVICE PERFORMANCE

This technology supports two core device types: a 25 Å gate oxide low leakage device (LP) for low power applications and an 18 Å high performance device (AP). Both devices make extensive use of halo implant and S/D engineering to meet the performance targets which are summarized in Table 3. Ion/Ioff for NMOS and PMOS devices are shown in Fig. 9. The LP NMOS and PMOS transistors meet 420/170 μA/um at 20 pA/μm leakage while the AP devices reach 920/400 μA/um at 20 nA/μm leakage. Data for the I/O devices is also shown in Fig. 9. Aggressive I/O performance is achievable while meeting intrinsic HCI reliability goals.

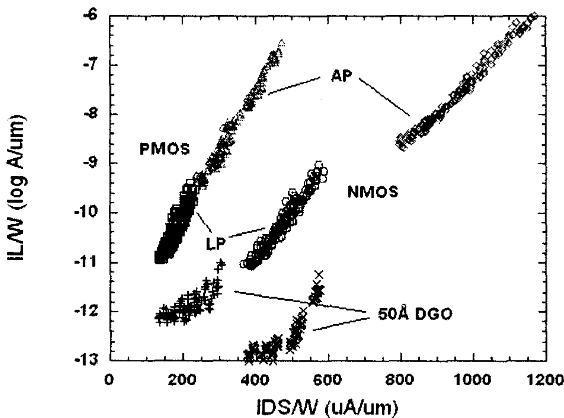


Fig. 9 Ion/Ioff curves for core and I/O devices

Table 3 Transistor Targets

Transistor Type	HiP8LP Target	HiP8AP Target	2.5V I/O	3.3V I/O
V_{DD} (V)	1.2	1.2 (1.0)	2.5	3.3
$T_{ox,\ optical}$ (nm)	2.5	1.8	5	7
L_{poly} (nm)	90	65	280	375
NMOS				
$T_{ox,\ inv}$ (nm)	3.1	2.4	5.5	7.3
I_{on} (μA/μm)	420	910(680)	575	570
I_{off} (nA/μm)	0.02	20 (10)	0.003	0.002
I_g (nA/μm)	0.002	3		
PMOS				
$T_{ox,\ inv}$ (nm)	3.2	2.5	5.6	7.4
I_{on} (μA/μm)	180	400(290)	250	250
I_{off} (nA/μm)	0.02	20 (10)	0.003	0.003
I_g (nA/μm)	0.0002	1		

To support SoC design methodology, a greater variety of device options is required. Controlling device leakage becomes a key goal of process technology when low voltage performance requirements dictate ever thinner gate oxides. In order for core circuit blocks to be utilized for both low power portable applications and high performance applications without extensive redesign, several process options must be available. These options include multiple gate oxide thicknesses on the same die [2,3], isolated well biasing schemes, and high Vt transistors. All three options are supported in our 0.10 μm process flow.

As an example we consider the triple gate oxide option. With gate oxides scaling in thickness below 20 Å, it becomes important to limit the gate tunneling current in certain blocks such as memories in order to meet standby current constraints. Therefore we offer the use of triple gate oxide (TGO) with the high performance device flow. Fig. 10 compares electrical Tox and gate leakage results for 50 Å I/O flows with (TGO) and without (DGO) the intermediate gate oxide. It is apparent that the intermediate gate oxide can be inserted with little impact to either the core gate oxide or I/O oxide thickness, and provides a reduction in gate leakage of three orders of magnitude.

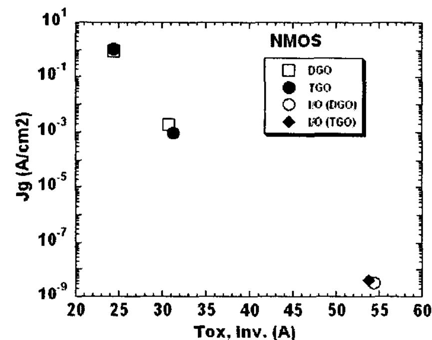
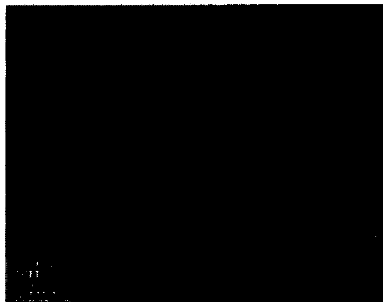
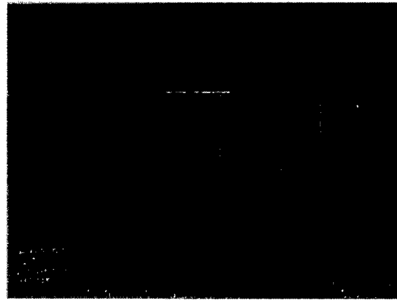


Fig. 10 NMOS gate leakage data





(a) (b)

Fig. 11 (a) Metal trench etch (b) via etch

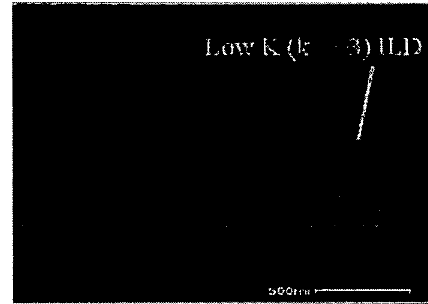


Fig. 12 Dual inlaid SEM. Final via size = 0.12 um

BACKEND

Both the new 193 nm resists and the use of low-k materials as interlevel dielectrics (ILD) pose significant challenges to the backend integration for 0.10 µm technologies. We are addressing these challenges through the utilization of a novel patterning strategy. This patterning strategy provides improved process capability and margin for the aggressive geometries and pitches specified for this technology node. Fig. 11 demonstrates this patterning capability for 0.30 µm pitch inlaid metal trenches and 0.12 µm sized inlaid vias etched into the low-k (k ~ 3) ILD. The minimum metal width is approximately 0.12 µm while the 0.10 µm diameter at the bottom of the via corresponds to an aspect ratio of ~ 6:1. With this integration we have produced yielding via chains with resistances in the range of 2 to 4 ohms/via as shown in Fig. 13. Excellent barrier step coverage and void-free copper fill of these structures is indicated from SEM cross-sections in Fig. 12 for vias with bottom diameters as small as 0.12 µm. The capability of the inlaid metal patterning and copper polish processes to maintain good electrical isolation at these geometries is evident in the line-to-line leakage data presented in Fig. 14 for 0.30 µm pitch features. The uniformity of the patterning and polish processes is also apparent from the sheet resistance data shown in Fig. 14 for 0.12 µm wide metal features.

CONCLUSIONS

A dense 0.10 µm technology has been developed incorporating dual inlaid Cu and low-k dielectric in the backend and 193 nm lithography at all critical levels. Two core devices along with a triple gate oxide option provide flexibility in meeting design constraints for power, performance, and leakage. Low-k interlevel dielectric and passivation layers help reduce the backend capacitance at the tight metal pitches of this technology node.

ACKNOWLEDGEMENTS

The authors thank and acknowledge the collaboration of our colleagues in process technology development in the Dan Noble Center. Management support from Bob Yeargain, Nick Kepler and Greg Bartlett is greatly appreciated.

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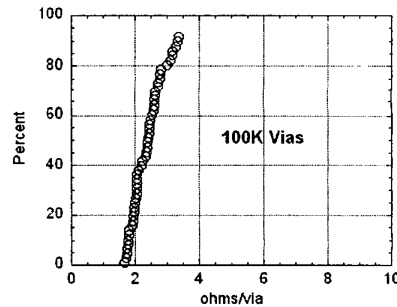

Fig. 13 M2-V1-M1 via chain yield

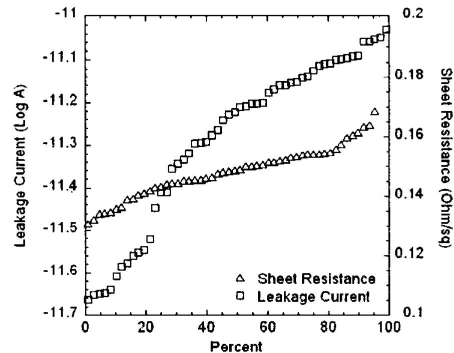

Fig. 14 Metal 1 snake/comb data for 0.30 µm pitch