Advanced SRAM Technology - The Race Between 4T and 6T Cells

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Abstract

This work discusses the trade-offs between 4T SRAM cells which use four bulk transistors (and have poly resistor or TFT loads) and 6T SRAM cells which use six bulk transistors (and use bulk PMOS loads). 4T SRAM cells have dominated the stand-alone SRAM market since first introduced in the 1970's, but 6T SRAM cells have been dominant for on-chip storage in advanced microprocessors and other logic circuits. However, recently there has been a resurgence of interest in 6T cells for stand alone SRAM applications. While 4T cells are typically smaller, they generally require a more complex process, and have poorer stability, especially at low voltage. This paper quantitatively examines several different trade-offs in SRAM cell design.

Process Complexity Trade-offs

The first major trade-off in SRAM cell design lies in the relationship between cell size and process complexity. Table 1 is a listing of various 4T and 6T SRAM cells which have been produced in Motorola and published in the literature[1-8]. Figure 1 is a plot of memory cell size vs. estimated process complexity for these SRAM cells. As can be seen, at a given feature size one can make a smaller cell by adding process steps. The memory cells shown divide into three basic types: 'Simple 6T' cells, which use a basic CMOS logic process; 'Advanced 6T' cells, which use process enhancements such as self-aligned contacts or local interconnect to reduce cell size; and 4T cells, which also typically have self-aligned contacts to reduce cell size. Although adding process steps of course increases the wafer cost, Figure 2 shows that a more complex process can still produce a less-expensive product if the increased number of good die more than compensates for the increased wafer cost. It is for this reason that most major SRAM manufacturers have been willing to add process complexity to reduce SRAM cell size.

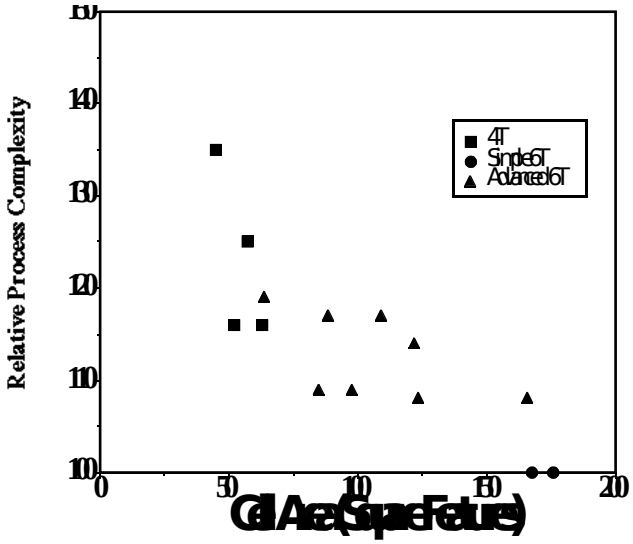

Figure 1: Comparison of SRAM cell size to estimated process complexity.

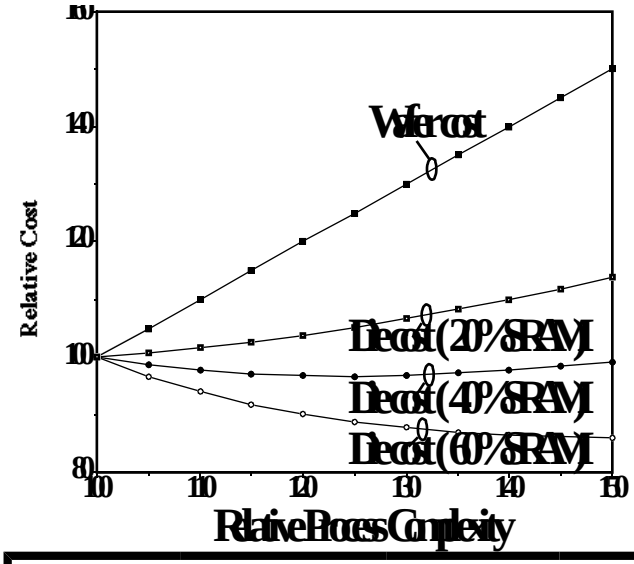

Figure 2: Estimated processing cost as a function of the process complexity from Figure 1.

Company	Type	Source	Features	Minimum Feature	Cell Area	Square Features	Relative Process Complexity
Motorola	Simple 6T	Internal	1 Poly 2 Metal	0.30µm	15.8µm2	175.6	100
Intel	Simple 6T	1994 IEDM	1 Poly 2 Metal	0.35µm	20.5µm2	167.3	100
Motorola	4T - Resistor	Internal	4 Poly - SAC 1 Metal	0.25µm	3.57 µm2	57.1	125
NEC	4T - Resistor	1996 VLSI	3 Poly - SAC 1 Metal	0.30µm	5.64 µm2	62.7	116
Hitachi	4T - TFT	1993 IEDM	5 Poly - SAC 1 Metal	0.40µm	7.16 µm2	44.8	135
Mitsubishi	4T - Resistor	1994 VLSI	3 Poly - SAC 1 Metal	0.40µm	8.36 µm2	52.2	116
Motorola	Advanced 6T	Internal	1 Poly LI+1 Metal	0.28 µm	9.7 µm2	123.7	108
Motorola	Advanced 6T	Internal	2 Poly - SAC 1 Metal	0.30µm	8.0 µm2	88.9	117
Motorola	Advanced 6T	Internal	1 Poly - SAC LI + 1 Metal	0.30µm	8.8 µm2	97.8	109
Sony	Advanced 6T	1996 VLSI	1 Poly - SAC LI + 2 Metal	0.28µm	5.01 µm2	63.9	119
IBM	Advanced 6T	1993 IEDM	1 Poly - SAC 2LI + 1 Metal	0.35µm	15.0 µm2	122.4	114
IBM	Advanced 6T	1993 IEDM	1 Poly LI + 2 Metal	0.45µm	33.6 µm2	165.9	109
Toshiba	Advanced 6T	1994 IEDM	2 Poly - SAC 1 Metal	0.30µm	7.65 µm2	85.0	109
Matsushita	Advanced 6T	1995 IEDM	1 Poly - SAC LI + 2 Metal	0.25µm	6.82 µm2	109.1	117

SAC = Self-Aligned Contact LI = Local Interconnect

Table 1: SRAM Cell Comparisons

Process Complexity Trade-offs

A second major trade-off in SRAM cell design is the issue of process commonality. Since it is often desirable to run SRAM and Logic processes in a

single wafer fab, having compatibility between SRAM and Logic processes is highly desirable. However, the process enhancements added to SRAM processes to improve cell size typically reduce the compatibility with Logic processes. A case in point is the use of self-aligned contacts. Figure 3 shows an SRAM cell bit line contact in a typical 4T cell using a self-aligned contact as compared to the same bit line contact in a Logic-compatible 'Simple 6T' cell. This basic incompatibility leads to many manufacturing issues when attempting to manufacture logic and SRAM in the same wafer fab line. Much of the effort aimed at developing 'Advanced 6T' SRAM cells has been motivated by the desire to address this basic incompatibility. However, as shown in Table 1, many of the published 'Advanced 6T' cells have

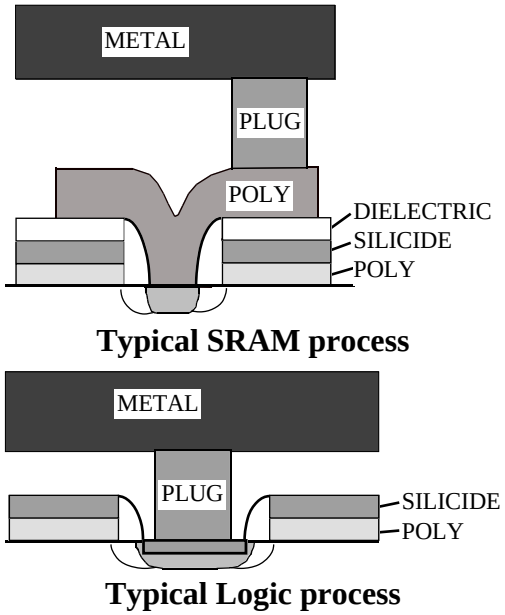

Figure 3: Process Comparison

maintained the use of the self-aligned contact due to the major benefit of reduced cell size.

Memory Cell Stability Trade-offs

The third major SRAM cell design trade-off lies in memory cell stability. Memory cell stability is typically characterized using Static Noise Margin (SNM). Figures 4 and 5 show plots of simulated SNM and cell read current vs. power supply voltage for 4T and 6T cells with three different cell ratios (ratio of NMOS storage device to NMOS access device).

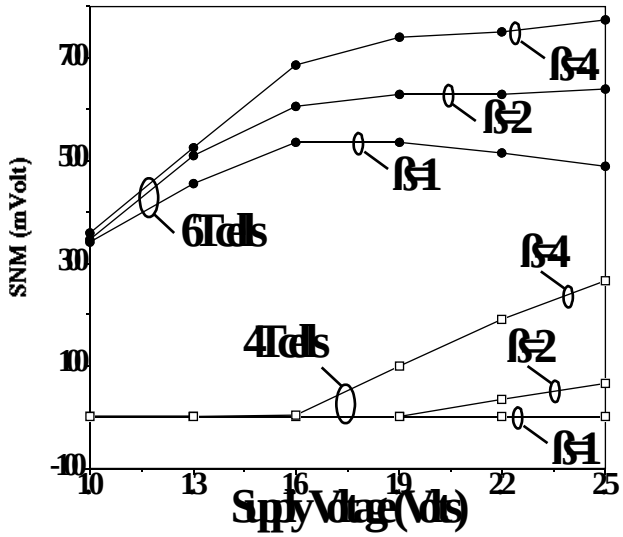

Figure 4: Simulated SNM for 4T and 6T cells vs cell ratio.

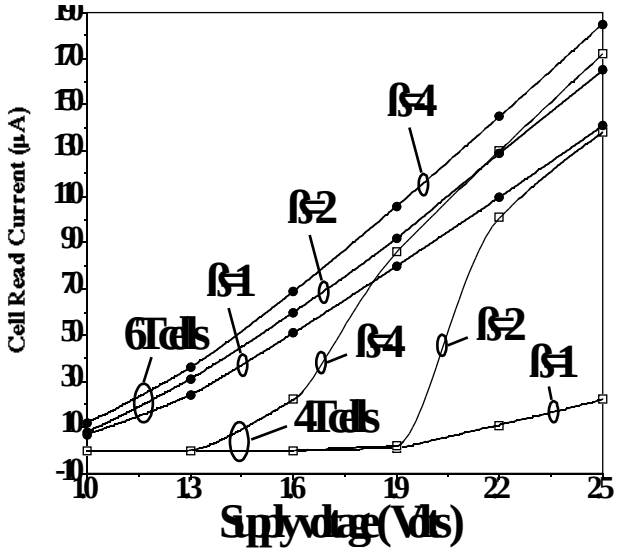

Figure 5: Simulated cell read current for 4T and 6T cells vs cell ratio.

As can be seen, 6T cells enjoy much better stability, especially at lower supply voltages. With a basic 4T cell, it is very difficult to scale much below a supply voltage of 2.5 volts. However, several enhancements which can prolong the useful life of 4T cells are shown in Figures 6 and 7, which again show simulated SNM and cell read current for several different cell designs. The use of a resistor fabricated using the LDD region [10]

increases the electrical cell ratio without increasing cell size. Boosting the word line voltage above the power supply voltage increases the high voltage written into the cell, improving both read current and SNM.

Figure 6: Simulated SNM for several enhanced 4T cells.

Figure 7: Simulated cell read current for several enhanced 4T cells.

Finally, the use of a 'strong' TFT (Ron = 1 Gohm) causes the 4T cell to begin to look like a 6T cell. In practice, however, building a manufacturable TFT with an on current large enough to improve cell stability has proven very difficult. Most TFT's used in manufacturing today are relatively weak devices which reduce standby current draw but do relatively little to improve memory cell stability. Because of the poorer cell stability at lower supply voltages of 4T cells, 4T cells have been forced to maintain higher cell ratios than 6T cells, eroding some of the cell size advantage that 4T cells have enjoyed. Because of this, recent 'Advanced 6T' cells have been able to approach very near to the cell sizes exhibited by 4T cells (as seen in Figure 1, especially Ref 5). The improved stability at low supply voltages is a major reason why the authors believe that 6T cells will become the dominant type of SRAM cell over the next several process generations, although continued enhancements to 4T cells will likely see them survive to at least 1.8 volts.

Soft-Error Rate Trade-offs

Finally, a fourth area of SRAM cell design consideration is the issue of Soft Error Rate (SER). Historically, 6T SRAM cells have been more robust with respect to soft errors than 4T cells [See, for example, Ref 9]. However, 6T SRAM cells have typically been significantly larger than 4T cells, thus storing significantly more charge. As 6T cells are scaled aggressively to smaller sizes and reduced voltages, SER will become a significant issue in 6T cells as well.

In conclusion, 4T SRAM cells, which have enjoyed nearly two decades of dominance of the SRAM market, appear to be very difficult to scale below the 1.8 volt power supply generation. Because of this, 6T cells will likely begin to dominate the stand-alone SRAM market as power supplies scale below 1.8 volts. This may lead to common process flows for advanced microprocessors and stand-alone SRAM products.

References

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