Soft Error Rate and Stored Charge Requirements in Advanced High-Density SRAMs

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Abstract

This work presents a quantitative model which attributes most soft errors in dense SRAMs not to alpha particles as is commonly accepted, but to cosmic ray events. This work also elucidates for the first time the stored charge required in SRAM cells to achieve acceptable soft error rates. Enhancements to add capacitance are necessary at the 4 Megabit level and beyond. One method of enhancing the cell capacitance is reported in detail.

Soft Error Rate Measurements

There are two generally accepted methods for monitoring soft error rate (SER) of semiconductor memories.

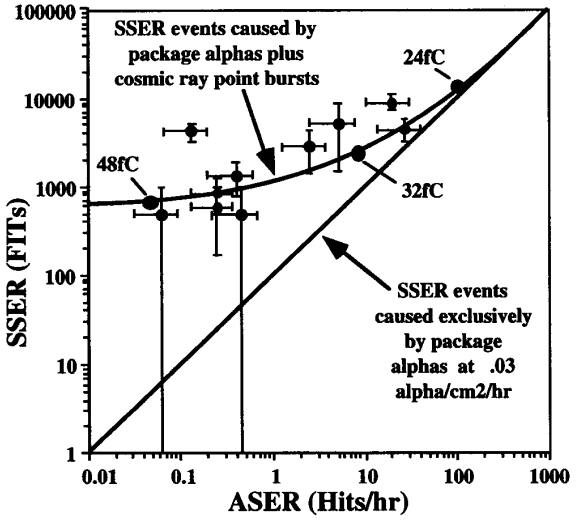

FIGURE 1
Correlation of Accelerated SER measurements with System SER measurements.

In Accelerated SER (ASER) measurements, memory circuits are exposed to a known flux of alpha particles, and the resulting soft errors are counted. In System SER (SSER) measurements, a large number of memory circuits are cycled for an extended time and the few soft-errors occurring are logged. It is generally assumed that alpha particles generated in the package or in the interconnect layers of the memory circuit are the cause of the SSER events. If this were so, a linear correlation between these two types of measurements would be expected. Figure 1 shows a correlation of ASER and SSER measurements over many different types of devices. These data represent more than 10 million device-hours of SSER testing. The data include 256K, 1 Megabit, and 4 Megabit SRAM circuits, and represent both CMOS and BiCMOS processes. It is important to note that some of the data are gathered at reduced supply voltages to increase the SER, and that the high SSER will not be seen at nominal operating voltages.

As can be seen, the assumption that alpha particles are the predominant source of the system soft errors provides a poor fit to the data. This discrepancy can be quantitatively explained by including in the SSER events the additional contribution of cosmic ray events. The occurrence of cosmic ray point bursts was calculated using cosmic ray flux data from Zeigler [1], and this data is reproduced in Figure 2. To generate the curve shown in Figure 1, a simple model is used to calculate the various components. Using alpha particle charge collection data and the cosmic ray flux data in Figure 2, the ASER and SSER values can be calculated as follows:

$$ASER = F_A \cdot A \cdot P(Q>Qcrit)$$

$$SSER = F_S \cdot A \cdot P(Q>Qcrit) + A \cdot D \cdot N(Q>Qcrit)$$

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F_A = alpha particle flux during ASER testing

F_S = alpha particle flux during SSER testing

A = memory array area

D = depth of point charge burst collection

P(Q>Qcrit) = probability of an alpha particle generating a charge Q, determined from charge collection (as in Figure 8)

N(Q>Qcrit) = number of events with charge Q, determined from Figure 2

The first term in the expression for SSER represents alpha particle induced events, and the second term represents cosmic ray induced events. Note that in this model the dominant event is when a cosmic ray derived high-energy neutron penetrates into the memory circuit and collides with a silicon nucleus to produce an energetic silicon nucleus, as shown in Figure 3. The depth of point charge burst charge collection has simply been assumed to be the distance between the bottom of the storage node and the bottom of the well, as shown in Figure 3. We believe these cosmic ray events have become the dominant type of soft error in advanced SRAMs, for two reasons. First, as device geometries have scaled down, doping concentrations have increased, reducing the funneling length of incident alpha particles, thereby reducing the charge collected from an incident alpha particle. Second, improvements in purity of semiconductor materials have reduced the flux of alpha particles in a typical circuit.

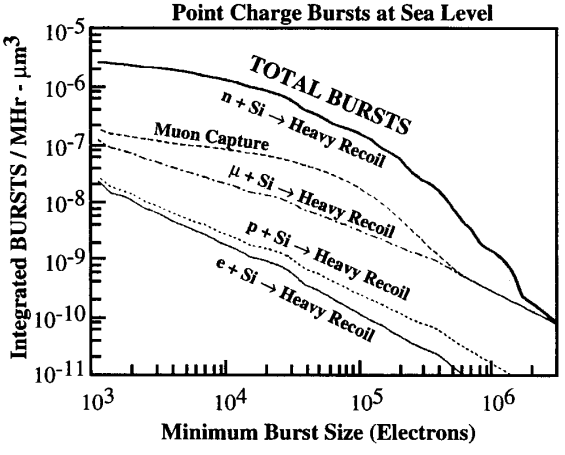

FIGURE 2
Rate of cosmic ray induced point bursts vs charge transfer (from [1]).

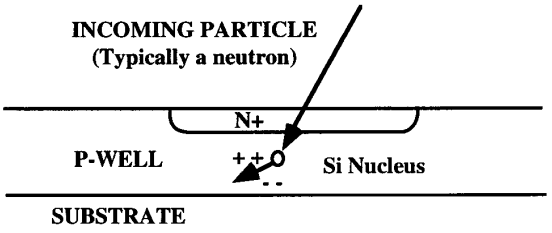

FIGURE 3
Schematic of silicon recoil event

Soft Errors in Memories

The only practical protection against these cosmic ray point charge bursts is to have sufficient stored charge to keep the rate of such events at an acceptable level. As memory densities have increased, cell capacitance has naturally decreased due to the decreasing size of the capacitive elements. Figure 4 shows a trend of memory cell capacitance for DRAM and SRAM cells *vs* memory density. DRAM cells have maintained a roughly constant cell capacitance through a variety of processing techniques. SRAM cells, however, have tended to allow cell capacitance to drop as the density has increased. Note that SRAM cell capacitances are typically far less than those of DRAMs. Because of the active nature of the SRAM cell, however, SRAM cells can sustain a disruptive event in which most of the stored charge is lost and still recover the correct data. For this reason, the critical charge to cause a soft error, shown in Figure 5, is more comparable between SRAMs and DRAMs. However, based on the SSER data from Figure 1, Figure 5 also shows that as SRAM scaling continues, enhancements to the SRAM cell to increase the stored charge are necessary at the 4 Megabit level and beyond. Based on the analysis in Figure 1, we believe that a cell critical charge of approximately 40 fC is necessary to ensure an acceptably low SSER of less than 1000 FITs.

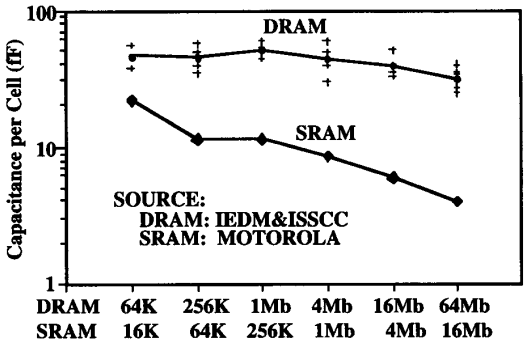

FIGURE 4
Capacitance trends for SRAMs and DRAMs

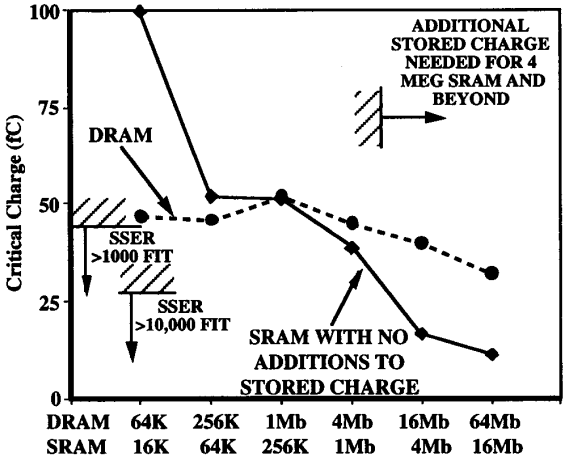

FIGURE 5
Critical Charge trends for SRAMs and DRAMs

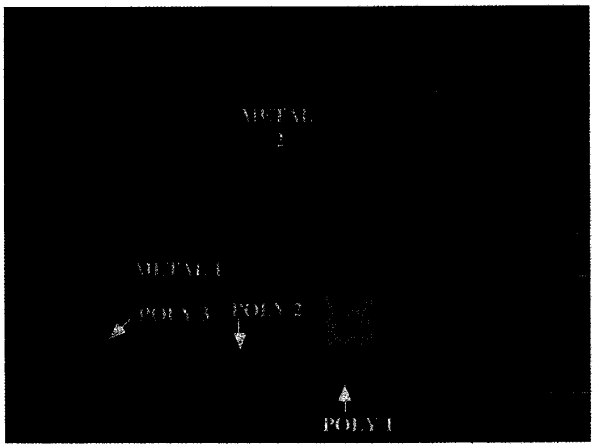

FIGURE 6
SEM cross-section of baseline 4 Meg BiCMOS process

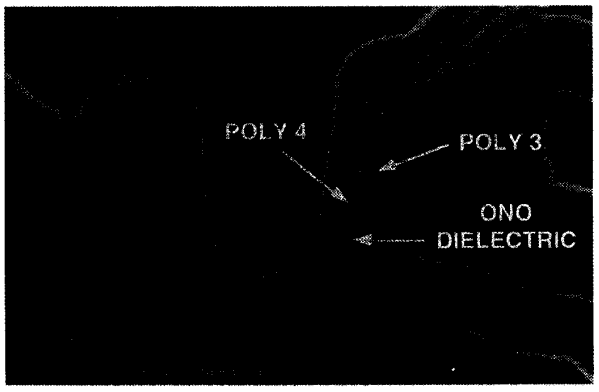

FIGURE 7
Stacked capacitor applied to 4 Meg SRAM

Adding Cell Capacitance

A simple method of increasing the stored charge is applied to a 4 Megabit high-speed BiCMOS SRAM [2]. In this cell, the third poly layer functions as a resistor load. To add capacitance, a thin dielectric is deposited on the third poly, and a fourth poly capacitor plate is deposited. A cross-section of the baseline 4 Meg BiCMOS process is shown in Figure 6. A cross-section of the added capacitor structure is shown in Figure 7. This capacitance approximately doubles the storage capacitance of the SRAM cell.

Charge Collection Measurements

Four Megabit SRAMs with several schemes to reduce alpha particle charge collection, with and without added capacitance, have been studied in detail. As has been discussed previously [3], alpha particle induced charge collection and measured ASER can be clearly related. Figure 8 shows alpha particle induced charge collection data for several different well structures on 4 Megabit BiCMOS SRAMs. Figure 9 shows ASER measurements on these same structures, including structures with enhanced capacitance. Figure 10 shows that by relating the slope of the charge collection data (in

decades/fC) to the slope of the ASER data (in decades/V), one can directly measure the cell capacitance and verify the increase in cell capacitance. This is the first time the charge collection measurements and ASER measurements have been correlated in this way to directly measure the storage node capacitance. Doubling the cell capacitance improved the measured ASER for a given well structure by 4 orders of magnitude, although, as discussed above and exhibited in Figure 1, the improvement in SSER is expected to be much smaller.

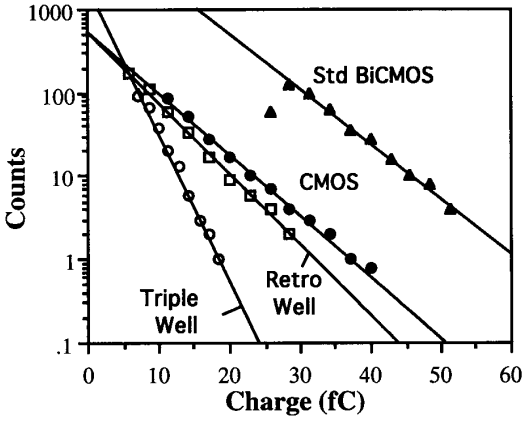

FIGURE 8
Charge collection results for 4 Megabit SRAMs with various well structures

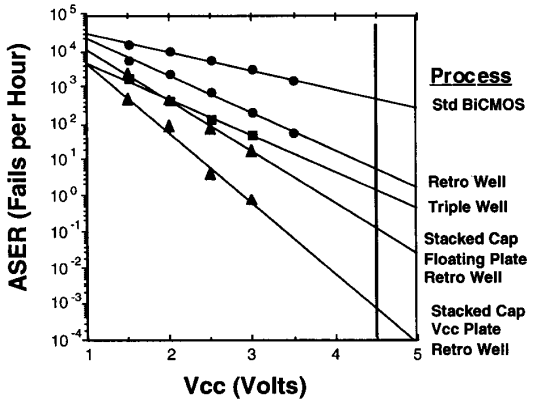

FIGURE 9
ASER results for 4 Megabit SRAMs with various well structures and enhanced capacitance

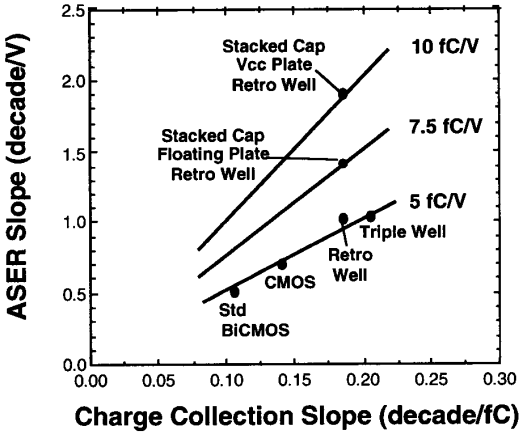

FIGURE 10
Cell capacitance measurement by correlating Charge collection with ASER.

Summary

In summary, a quantitative model is presented showing that cosmic ray events are the dominant cause of soft errors in dense SRAMs. The stored charge requirements in SRAM cells to achieve acceptable soft error rates are elucidated for the first time. One method of increasing SRAM cell capacitance, that of adding a poly capacitor plate, is reported in detail.

References

[1] Ziegler, et.al., "The Effect of Sea Level Cosmic Rays on Electronic Devices", *J. Appl. Phys.*, **52**(6), pp. 4305-4312, June, 1981.

[2] Hayden,et.al., "A High-Performance 0.5 µm BiCMOS Technology for Fast 4-Mb SRAMs", *IEEE Trans. Elect. Dev.*, **39**(7), pp.1669-1679, July, 1992.

[3] Burnett,et.al., "Soft-Error-Rate Improvement in Advanced BiCMOS SRAMs", *IEEE IRPS Proceedings*, pp.156-160, April, 1993.

[4] Olsen, et.al., "Neutron-Induced Single Event Upsets in Static RAMs Observed at 10km Flight Altitude", *IEEE Trans. Nucl. Sci.*, **40**(2), pp.74-77, April, 1993.