POLY EMITTER BIPOLAR HOT CARRIER EFFECTS IN AN ADVANCED BICMOS TECHNOLOGY

S.P. Joshi, R. Lahri and C. Lage

Fairchild Semiconductor, Memory Products Division
Puyallup, WA 98373

ABSTRACT

Hot carrier effects due to reverse biasing of emitter-base junction in a poly emitter bipolar transistor are discussed. Degradation of transistor current gain under DC, pulsed DC and AC stress conditions is found to be determined by the total injected charge through the reverse biased junction. These results coupled with the design simulations are used to predict the reliability of bipolar devices in a BiCMOS circuit.

INTRODUCTION

Reverse biasing of the emitter base junction is known to degrade the current gain (beta) of a bipolar transistor. This condition is more likely to occur in a BiCMOS circuit, where bipolar and CMOS gates are frequently interfaced. There are several design and reliability issues which are unique to the scaled bipolar devices (1). When bipolar transistors are scaled-down shallow junctions and heavy doping density in the lateral and vertical dimensions become imperative. Higher electric fields, which are frequently encountered between emitter and extrinsic base regions, can severely accelerate hot carrier induced beta degradation. Several studies have been reported in the past to explain avalanche / hot carrier induced junction degradation (2-6). However, very limited information is available about the hot carrier effects on scaled-down bipolar devices (7,8). In particular, beta degradation is not well quantified making it virtually impossible to predict device lifetime in a given circuit. Figure 1 (inset) shows a typical BiCMOS inverter in which CMOS gates and bipolar drivers are interfaced. HSPICE simulation indicates that E-B junction of transistor Q1 can be reverse biased during switching (Figure 1). Though it is a transient phenomenon the stress on this transistor can be significant when the inverter is operating at a very high frequency (100 MHz or above). This investigation is directed towards the quantification of beta degradation under DC, pulsed DC and AC stress conditions in order to be able to predict the reliability of polysilicon emitter transistor Q1.

EXPERIMENTAL

Poly emitter transistors are fabricated by the one micron BiCMOS III process (9). The process sequence involves twin buried layers, 1.5 μm epi, double poly and two level metal. Boron implants are used to form intrinsic and extrinsic base regions. The emitter window is opened in the interpoly dielectric prior to poly2 deposition. N++ doped poly2 is used as an emitter cap for the bipolar transistors (Figure 2). Transistor beta degradation is studied using an automated stress and measurement test set-up. In this computer controlled system Emitter-Base (E-B) junction of a bipolar transistor can be stressed under DC, pulsed DC and AC conditions. HP4145 semiconductor parameter analyzer is used for constant current / voltage stress and device parameter extraction. Pulsed DC and AC stress voltages are derived from HP8112A pulse generator. The device under test is stressed in decade increment of time and transistor beta as a function of collector current is recorded after each stress duration. The extended temperature (-55°C to 175°C) tests are performed on ceramic packaged devices.

RESULTS & DISCUSSION

Constant voltage stressing results indicate that beta degradation, for a fixed stress duration, increases with increasing reverse bias accross the E-B junction. As shown in Figure 3 this degradation in beta is not limited to low collector current levels (Ic=10uA) and can extend to higher current levels (Ic=1mA). With increasing reverse voltage level an increasingly large amount of current flows through the E-B junction. This reverse current which is primarily confined tc emitter perimeter region under the influence o; localised electrical field (Figure 4) can generat hot carriers. These hot carriers in turn can damage Si-SiO2 interface by increasing interfacial trap density and if energetic enough they surmount Si-SiO2 barrier giving rise to an increase in fixed oxide charge density and oxide trap charge density. In the forward transistor operation mode, beta degrades because of increased recombination-generation in the space charge region(4). Figure 5 shows an increase in reverse current, due to generation- recombination centers,

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after stress. Gummel plots also indicate that emitter-base ideality factor (n) first increases from 1 to 2 for lower levels of IB and subsequently for the entire range of IB up to Gummel knee current (Figure 6). In this study ideality factor does not exceed 2 as observed by other investigators (1) thereby indicating that recombination-generation remains the predominant degradation mechanism. When the stressed transistors are annealed in forming gas for 2 hours at 200 C recovery in beta to the extent of 10-15% was observed (Figure 7). The recovery is found to saturate as increasing the annealing time to 10 hours did not improve beta any further. Similarly, a forward current soak at room temperature also resulted in recovering beta by 10%.

Constant voltage stress results (Figure 3) ,however, have very limited application for predicting device lifetime. Since, reverse current voltage characteristics of the E-B junction is a strong function of temperature, stress analysis for extended temperature operation becomes increasingly difficult. Reverse stress current is thus controlled. Constant current (CC) stressing of the reverse biased E-B junction reveals that beta degradation depends on stress current (IR) and stress duration. An excellent correlation is observed between stress charge and beta degradation (Figure 8). The most striking feature of the curve (Figure 8) is its validity for six orders of stress current magnitude. These results also show that beta degradation is independent of power in 3.6E-9 W to 5.6E-3 W range. Beta degradation in a simplified form thus can be expressed as:

$$dB/B = K1 \, Log(QR) + K2 \quad ; \quad QR > Qcrit \quad .. (1)$$

This "Charge to degradation" concept will be subsequently used to predict device lifetime in a specific circuit operating condition. K1, K2 and Qcrit in Equation 1 are constants for a particular device design and at best can be determined experimentally. The curve in Figure 8 can be divided in two regions. In the initial stages of stressing (Region I) interface traps play a major role in beta degradation. These traps being donor type are positively charged when empty . These donor type traps in conjunction with initial positive fixed oxide charges can deplete the surface of underlying P-type extrinsic base region. This increases recombination in the surface space charge region resulting in beta degradation. This trend continues upto a critical charge (Qcrit) and the degradation up to Qcrit can be described as soft degradation as beta can be recovered by forward current soak at room temperature or annealing at elevated temperatures. During the forward current soak electrons can occupy these donor type interfacial traps making them neutral. Similarly, some of the positive fixed charge in the immediate vicinity of Si-SiO2 interface can also be neutralised/ compensated by low energy electrons leading to beta recovery. Beyond Qcrit (Region II) a non-saturating type of degradation can be sustained only if more and more traps are generated over a wider surface region widening the surface space charge region. A reduction in zero bias E-B capacitance after reverse stress was experimentally verified supporting the above model. Extended temperature (-55 C to 175 C) constant current stressing results indicate that temperature coefficient of beta degradation increases with decreasing temperature which is typical of hot carrier effects. Temperature coefficient of beta degradation was found to be -2560 ppm/C in the above mentioned temperature range with corresponding activation energy of -.02 eV. Therefore, room temperature CC stress results can be extended to -55 °C to 175 °C without much loss of accuracy.

Significance of Qcrit can be best understood by comparing beta degradation under DC, pulsed DC and AC stress conditions. As can be seen (Figure 9) that degradation under DC and pulsed DC conditions is equivalent, for a given stress charge, confirming the model that the total reverse stress charge determines the beta degradation. Under AC condition, however, degradation is considerably reduced indicating that forward current soak reduces the positive charge build-up near E-B perimeter and beta integrity is preserved longer.

Since, beta degradation depends on the cumulative stress charge through reverse biased E-B junction it should be possible to predict device lifetime using beta degradation vs stress charge curves (Figures 8 & 9). Figure 10 shows the relation between device lifetime and permissible beta degradation for poly emitter bipolar transistor (Q1) operating at 100 MHz (100 Mb/S). The calculations are based on charge to degradation model and HSPICE simulation results which indicate that reverse charge of 9.89E-19 C can flow through E-B junction every cycle. The calculations of lifetime based on DC stress measurements, though not representative, provide the lower bound for lifetime. The projected device lifetime based on AC stressing is more representative of real device operation situation.

CONCLUSIONS

In this paper reverse biasing of emitter-base junction of poly emitter transistor in a BiCMOS circuit and effects of hot carriers on transistor gain are discussed. Beta degradation behavior of poly emitter transistor under DC, pulsed DC and AC stress conditions is quantified. It is demonstrated that beta degradation depends on the total injected charge through the reverse biased emitter-base junction. The experimental results coupled with "charge to degradation" model and circuit simulations are used to predict the reliability of a bipolar device in a BiCMOS inverter circuit.

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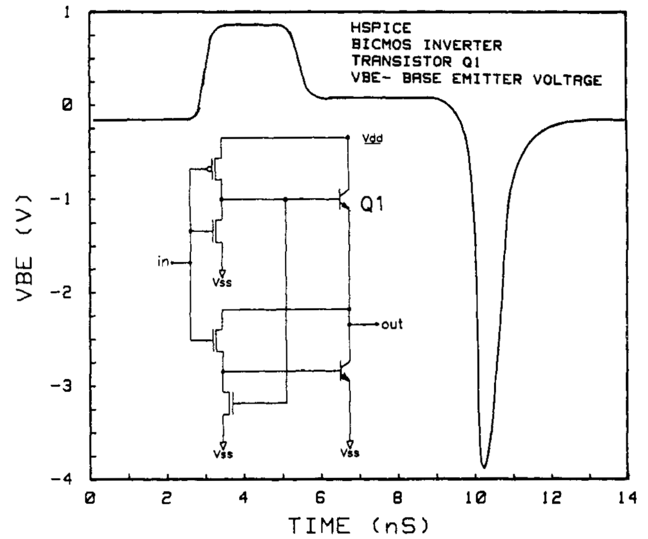
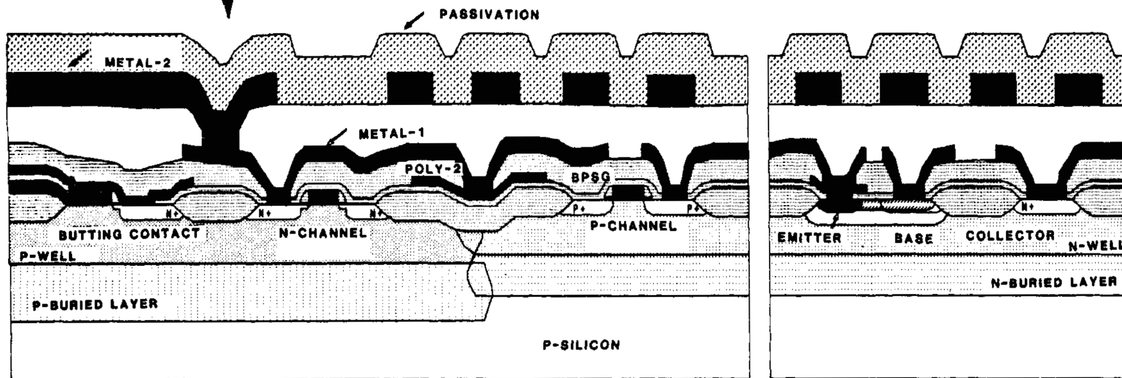


FIGURE 1
BiCMOS inverter (in-set) and HSPICE simulation results of voltage across E-B junction of Q1.

FIGURE 2
Schematic cross section of the devices in BiCMOS III process.



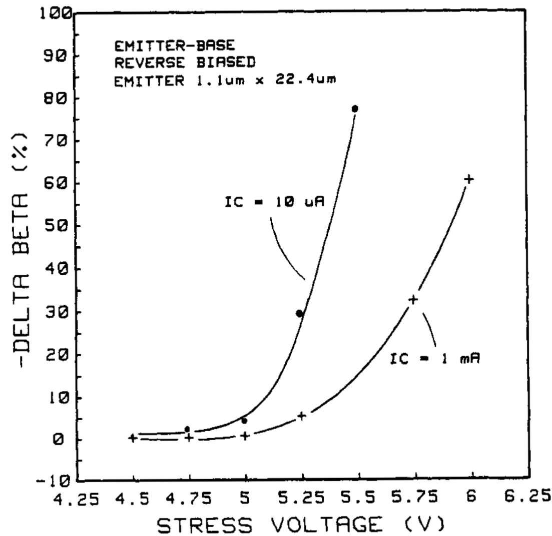


FIGURE 3
Effect of constant voltage stress on beta of poly emmiter transistor.

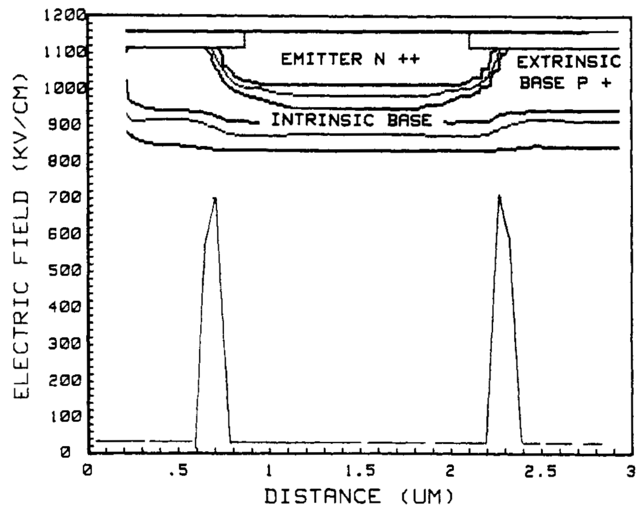


FIGURE 4
PISCES simulation of reverse biased (5 V) E-B junction indicating localised high electric field regions.

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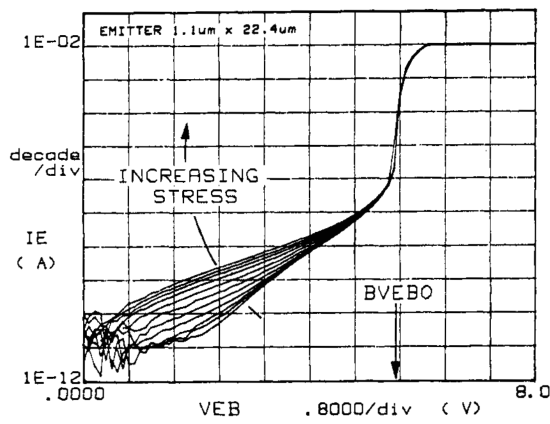

FIGURE 5
Effect of stressing on the reverse current-voltage characteristics of E-B junction.

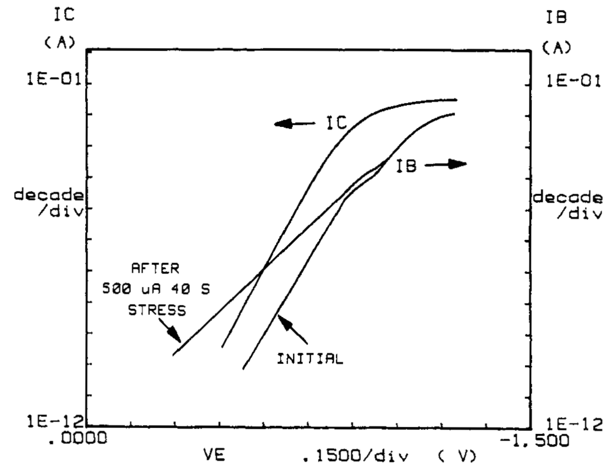

FIGURE 6
Gummel plots for a poly-emitter bipolar transistor before and after stress.

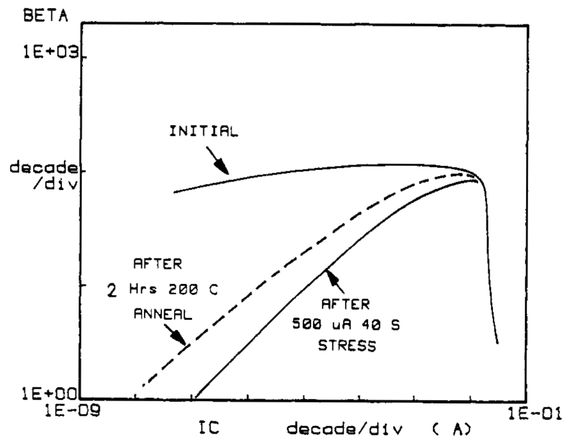

FIGURE 7
Pre and post stress beta as a function of collector current.

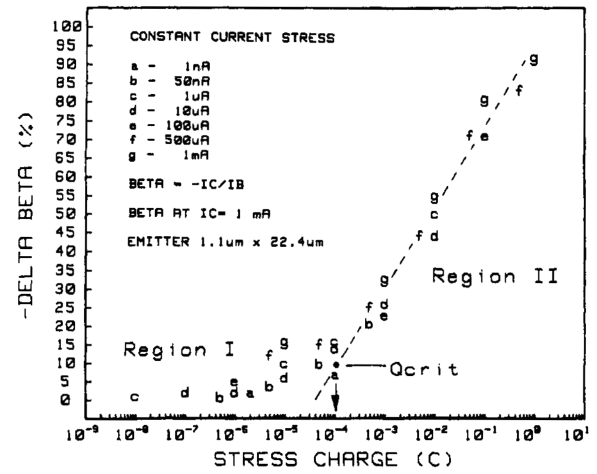

FIGURE 8
Dependence of beta degradation on reverse stress charge for poly emitter transistor.

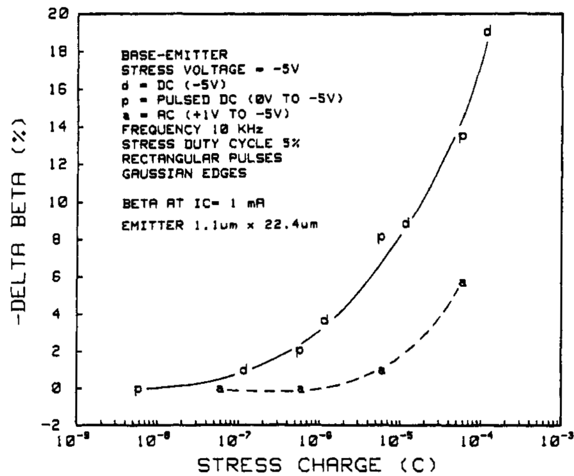

FIGURE 9
Summary of DC, pulsed DC and AC stress conditions on beta degradation.

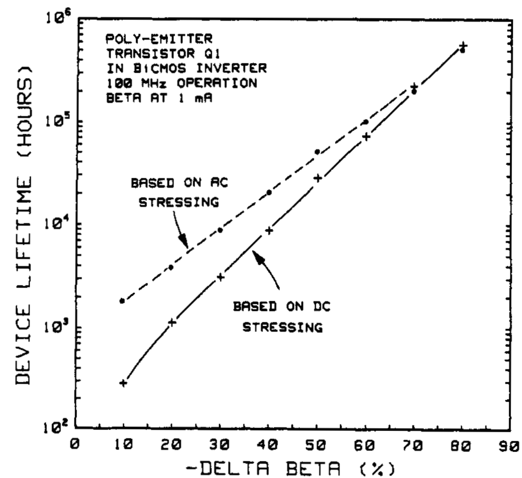

FIGURE 10
Device lifetime projections for poly emmiter transistor Q1.