A Quadruple Well, Quadruple Polysilicon BiCMOS Process for Fast 16 Mb SRAM's

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***Abstract*— An advanced, high-performance, quadruple well, quadruple polysilicon BiCMOS technology has been developed for fast 16 Mb SRAM's. A split word-line bitcell architecture, using four levels of polysilicon and two self-aligned contacts, achieves a cell area of 8.61 μm^2 with conventional I-line lithography and 7.32 μm^2 with I-line plus phase-shift or with deep UV lithography. The process features PELOX isolation to provide a 1.0 μm active pitch, MOSFET transistors designed for a 0.80 μm gate poly pitch, a double polysilicon bipolar transistor with aggressively scaled parasitics, and a thin-film polysilicon transistor to enhance bitcell stability. A quadruple-well structure improves soft error rate (SER) and allows simultaneous optimization of MOSFET and bipolar performance.**

I. Introduction

FAST, high density static RAM's require both a small, stable bitcell and a high performance process. At the 16 Mb generation, a bitcell area of less than 9.0 μm^2 is required in order to meet packing density and package constraints. This can be achieved using I-line lithography with multiple layers of polysilicon to accomplish the various bitcell functions and multiple self-aligned contacts to further increase packing density. Use of I-line plus phase-shift or deep UV lithography provides for even smaller bitcell areas. With the scaling of power supply voltage and bitcell area, cell stability becomes of increasing importance. A symmetrical split word-line bitcell layout [1], [2] and thin film PMOS polysilicon transistors (TFT's) as SRAM loads have been introduced in order to enhance cell stability. Speed or access time requirements are met by adding a high performance, double polysilicon bipolar transistor [3]. With careful design, bipolar parasitic capacitances can be further reduced without an increase in process complexity [4]. With the aggressive scaling of bitcell areas at the 4 Mb generation and beyond, soft error rate has become a primary reliability concern for SRAM's [5], [6]. In this technology, a quadruple-well has been developed to provide diode isolation for the memory array while allowing for simultaneous optimization of MOSFET and bipolar transistors.

II. Process Technology

A schematic cross section of the quadruple well, quadruple polysilicon, double-level metal BiCMOS technology is shown in Fig. 1. Table I is an outline of the process flow and Table II summarizes process parameters. Major device parameters are presented in Table III. This CMOS-based BiCMOS technology uses triple buried layer and triple well implants, resulting in four distinct well regions: bipolar, PMOS, peripheral NMOS, and array. SER considerations dictate a diode isolated array, but the thinner epi required by bipolar scaling forces the introduction of a separate array buried layer. A grown epitaxial layer thickness of 1.6 μm gives a final flat zone width of approximately 0.40 μm. Separate n-well and collector regions are required to meet MOSFET punchthrough and bipolar breakdown requirements. A split well drive technology eliminates the need for chan-stop implants and reduces MOSFET narrow-width effects [7]. PELOX or poly-encapsulated LOCOS provides field isolation [8]. Surface channel NMOS and buried channel PMOS transistors are fabricated with a

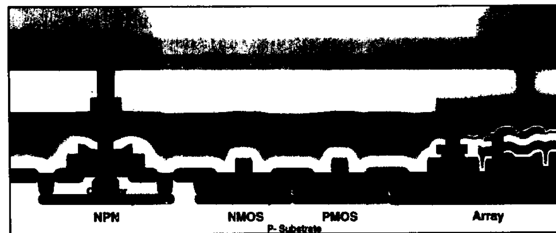

Fig. 1. Schematic cross section of quadruple well, quadruple poly BiCMOS technology for fast 16 Mb SRAM's.

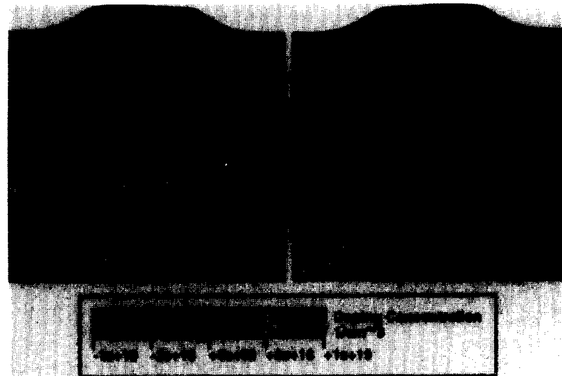

Fig. 2. Results of two dimensional process (SUPREM-4) simulation of the quadruple well structure. The figure presents doping contours at the edge of the array and peripheral p-wells.

Manuscript received October 28, 1993; revised May 20, 1994. The review of this paper was arranged by Associate Editor D. A. Antoniadis.

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IEEE Log Number 9405900.

0018-9383/94$04.00 © 1994 IEEE

TABLE I
SIMPLIFIED PROCESS FLOW

Process step
buried layer implants
epitaxial layer growth
well implants
first well drive
isolation patterning
field oxidation
sacrifical oxidation
second well drive
gate oxidation
threshold implants
gate stack formation
gate patterning
LDD implants
spacer information
source/drain and base implants
first interpoly dielectric
emitter poly deposition
emitter poly patterning
second interpoly dielectric
TFT gate poly deposiiton
TFT gate poly patterning
TFT gate dielectric
TFT channel poly deposition
TFT channel poly patterning
TFT source/drain implant
first interlevel dielectric
contact patterning
contact plug formation
metal-1 deposition
metal-1 patterning
second interlevel dielectric
via patterning
via plug formation
metal-2 deposition
metal-2 patterning
via plug formation
passivation

TABLE II
PROCESS PARAMETERS

General Technology	Quadruple well BiCMOS
	Quadruple-Level Poly
	Double-level Metal
	Tungsten plugs at contact and via
Gate Oxide	105 Å
Isolation	1.0 μm pitch
	0.60 μm break-to-break isolation
	0.40 μ, channel width
MOSFET	0.80 μm poly-1 pitch
	0.40 μm poly gate length
	800 Å spacers
Bipolar	Double poly, E-B-C self-aligned
	0.40 × 1.2 μm emitter area
TFT	undergrated PMOS TFT
	0.40/0.80 W/L
	0.35 μm gate-to-drain offset
Contact	0.45 × 0.45 μm
Metal-1	0.55/0.50 μm
Via	0.50 × 0.50 μm

TABLE III
DEVICE PARAMETERS

MOSFET		
	V_T (N/P)	0.80 V/-0.95 V
	I_{DS} (N/P)	360 μA/μm/180 μA/μm
Bipolar		
	Beta	135
	BV_{EBO}	5.4 V
	BV_{CBO}	21 V
	BV_{CEO}	4.6 V
	C_{BC}	5.0 fF
	C_{CS}	8.8 fF
TFT		
	on/off ratio	$1*10^5$

105 Å gate oxide and 800 Å silicon nitride spacers. Double polysilicon, emitter-base-collector (E-B-C) self-aligned NPN bipolar transistors with aggressively scaled parasitics have been added to meet speed requirements. Undergated PMOS TFT's are used as SRAM loads in order to improve cell stability. In this quadruple poly process, the first polysilicon layer forms the MOSFET gates and the bipolar extrinsic base; the second is used for the bipolar emitter, the first self-aligned contact, and a local interconnect; the third poly forms the second self-aligned contact and the TFT gate; while the fourth layer is used for the TFT channel. The first and second polysilicon layers are strapped with WSi_x and $TiSi_2$, respectively, giving sheet resistances of 10 and 2Ω/square. Two self-aligned contacts are employed to reduce bitcell area. Tungsten plugs are used at contact and via [9]. Stacked contacts and vias as well as headless contacts are employed. Two levels of aluminum copper (AlCu) metallization are employed. Planarization prior to both metal layers is by a standard resist etchback (REB) approach [10]. Conventional I-line lithography is used to achieve pitches of 1.0, 0.8, and 1.05 μm at active, gate poly, and metal-1 respectively; 0.45 × 0.45 μm bit-line contacts; and 0.50 × 0.50 μm vias. This technology is designed for a power supply voltage of 3.3 V.

Fig. 3. SEM cross section through SRAM bitcell showing 0.35 μm transfer device, formed using PELOX isolation.

III. DEVICE CHARACTERISTICS

A. Quadruple Well Design

A diode isolated array is used in this technology to provide protection against alpha particle events and to allow the option of applying a back-bias to the array. A junction under the array cuts off alpha particle funneling tails and reduces the charge collected at the storage node after an SER event. In

Fig. 4. TEM cross section of bird's beak formed using PELOX isolation.

designing this process, it was found that the requirements for the buried layers under the array and the bipolar differ. Placing the bipolar buried layer under the array increases the risk of vertical punchthrough and snapback. Consequently, two different n-type buried layers are required. The p-type buried layer serves to provide isolation and compensate for arsenic autodoping during epi growth. It has also been found that unlike the previous generation, for a 0.35 μm technology, the doping requirements for the nwell and the collector are beginning to again diverge. Placing a bipolar in an n-well with sufficient doping to suppress PMOS punchthrough would result in an unacceptable degradation in base-collector breakdown. A split-well drive is used in our process where a portion of the well drive occurs after field oxide growth. This eliminates the need for chan-stop implants while reducing the narrow width effect. The quadruple well structure was optimized using two dimensional process (SUPREM-4) and device (PISCES-2B) simulation. Fig. 2 presents the results of SUPREM-4 simulations, depicting the well structure and doping contours at the edge of the array and peripheral p-wells. The quadruple well was designed to prevent punchthrough between the n^+ source/drain and array buried layer as well as between the array p-well and the p-type substrate. Good electrical connection to the array buried layer from the adjacent n-well is also achieved.

B. Isolation

PELOX [8], or poly-encapsulated local oxidation of silicon, is used to achieve an active pitch of 1.0 μm, with a nominal final or physical line and space of 0.40 and 0.60 μm, respectively. Fig. 3 is an SEM cross section through the bitcell showing a 0.35 μm transfer gate. A very sharp bird's beak as well as a nearly planar topography are apparent. PELOX achieves an encroachment of approximately 0.10 μm/side. Fig. 4 is a TEM cross section of the final PELOX bird's beak structure. This figure demonstrates that there is no evidence of gate oxide thinning nor any silicon defects at the active edge. PELOX provides electrical isolation for a beak-to-beak field isolation space as small as 0.55 μm, as illustrated in Fig. 5. The steep bird's beak profile of PELOX and the split well drive process serve to suppress the narrow width effect for MOSFET's with physical widths as small as 0.30 μm, as shown in Fig. 6. Finally, it has been demonstrated that PELOX does not degrade gate oxide integrity and diode quality relative to conventional LOCOS and poly-buffered LOCOS (PBL) technologies.

C. MOSFET's

In this technology, surface channel NMOS and buried channel PMOS transistors have been used to maintain process simplicity. Drive current was optimized while ensuring an adequate lifetime under hot-carrier stress and an off-leakage due to punchthrough, drain-induced barrier lowering (DIBL), and GIDL (gate-induced drain current) of less than 0.1 and 1.0 pA/μm of device width for NMOS and PMOS transistors, respectively. The transistor design provides long channel behavior to a minimum physical gate length of 0.30 μm. Device characteristics for NMOS and PMOS devices are pre-

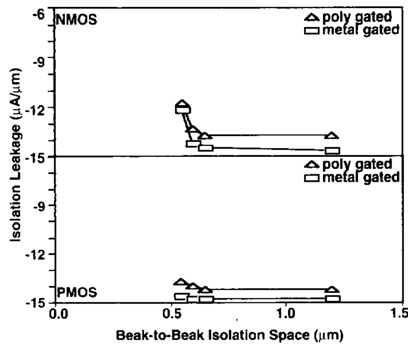


Fig. 5. Electrical isolation as a function of isolation space. Off-leakage of a gated isolation space versus beak-to-beak isolation space. Data included for both polysilicon and metal gated structures.

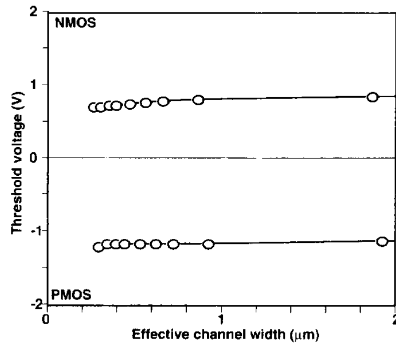


Fig. 6. NMOS and PMOS threshold voltage as a function of effective channel width, demonstrating the reduction in narrow width effect achieved with PELOX isolation plus a split well drive.

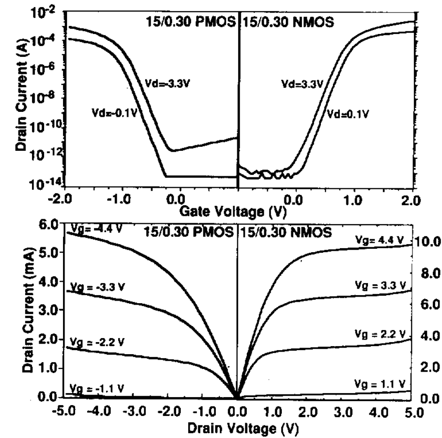


Fig. 7. Subthreshold turn-on characteristics (top) and drain current characteristics (bottom) for NMOS and PMOS transistors with 0.30 μm poly gate lengths.

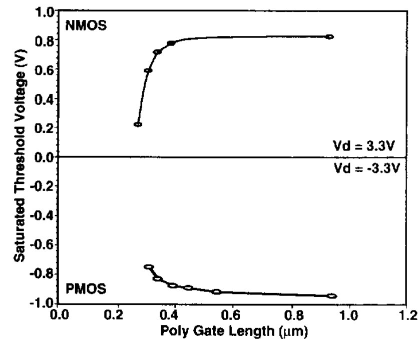


Fig. 8. NMOS and PMOS saturated threshold voltage as a function of poly gate length. Threshold measured at 3.3 V drain-source voltage.

sented in Fig. 7. The subthreshold characteristics demonstrate that MOSFET off-current has been held to below 0.10 and 1.0 pA/μm of device width for NMOS and PMOS transistors, respectively. Achieving such low off-current values requires some tradeoffs in on-current. From the drain current characteristics, it is seen that the nominal drive current achieved is 360 and 180 $\mu A/\mu$m for NMOS and PMOS, respectively. Fig. 8 is a plot of threshold voltage versus poly gate length, confirming adequate long-channel behavior to a gate length of 0.30 μm. The MOSFET's have been designed to support a gate poly pitch of 0.80 μm as well as scaled self-aligned contacts and double polysilicon bipolar transistors. This has necessitated reducing the spacer thickness to 800 Å. The choice of the spacer width and composition has been found to have significant impact on NMOS hot carrier resistance [11]. One of the primary issues associated with scaling spacer thickness is controlling PMOS short channel effects and GIDL [11]. Integration of subsequent polysilicon layers required for the bitcell and the bipolar and thin film polysilicon transistors was shown to have relatively little effect on bulk MOSFET performance.

D. Bipolars

Double polysilicon NPN bipolar transistors are introduced to provide improved circuit performance [3]. The double poly

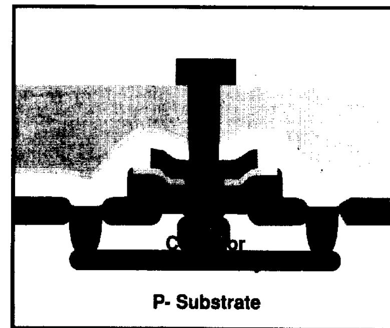


Fig. 9. Schematic cross section of double polysilicon NPN bipolar transistor showing selectively compensated collector region and pull back of p-well from collector edge.

structure reduces collector-base capacitance (C_{CB}) and base resistance (R_B) relative to the previous generation 4 Mb process which employed a single polysilicon, nonself-aligned device [12]. To optimize bipolar speed for ECL-like signal paths, parasitic capacitances have been aggressively scaled

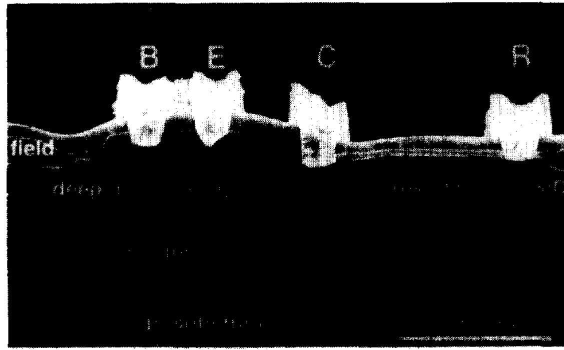


Fig. 10. SEM cross section of double polysilicon NPN bipolar transistor along with merged n-ECL resistor.

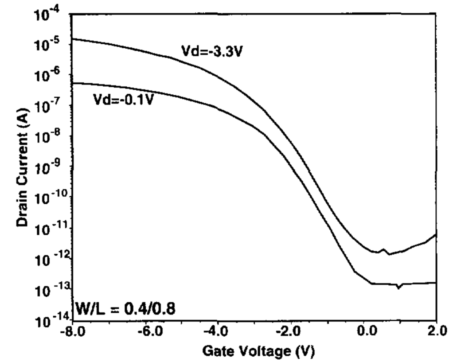


Fig. 13. Turn-on characteristics for a 0.4/0.8 undergated PMOS TFT.

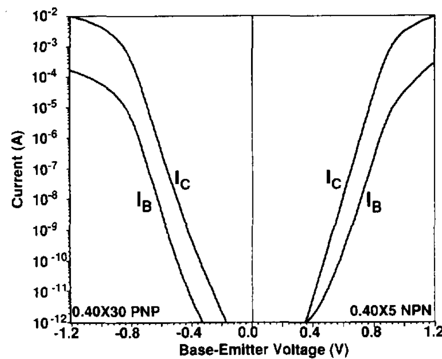


Fig. 11. Gummel characteristics for 0.4×5.0 NPN and 0.4×30 PNP double polysilicon bipolar transistors.

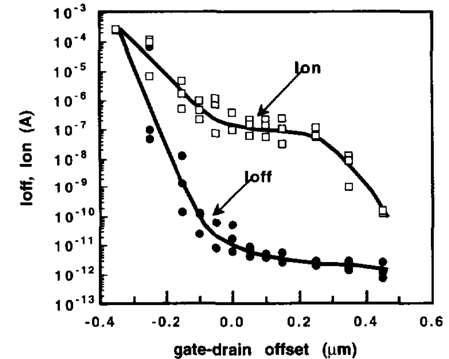


Fig. 14. TFT on- and off-current as a function of gate-to-drain offset for a 0.4/0.8 undergated PMOS TFT. On-current measured at $V_{DS} = V_{GS} = 3.3$ V and off-current at $V_{DS} = 3.3$ V, $V_{GS} = 0$ V.

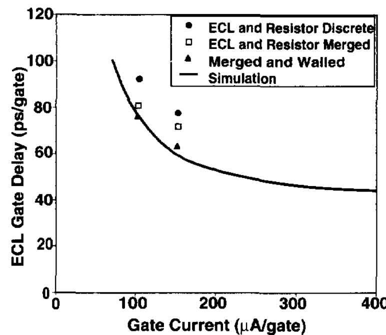


Fig. 12. Simulated and measured ECL gate delay as a function of switching current for 0.4×1.2 NPN bipolar transistors. Plot compares delays for the discrete SCC bipolar and ECL resistor combination, the merged implementation, and the merged implementation with a walled emitter.

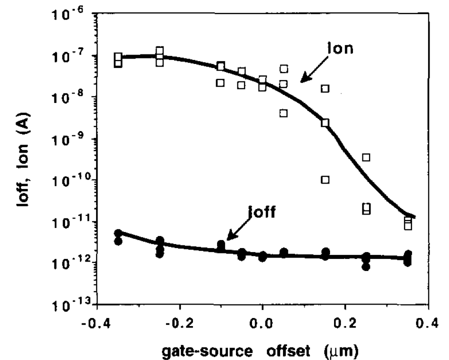


Fig. 15. TFT on- and off-current as a function of gate-to-source underlap for a 0.4/0.8 undergated PMOS TFT. On-current measured at $V_{DS} = V_{GS} = 3.3$ V and off-current at $V_{DS} = 3.3$ V, $V_{GS} = 0$ V.

by using a selectively compensated collector (SCC) and by pulling the p-well and p^+ buried layer away from the bipolar edge [4]. In the SCC approach, the collector region is lightly p-type doped, except for a moderately doped n-type pocket implanted through the emitter window. Hence, the collector is now self-aligned relative to the base and emitter. The onset of base pushout is delayed while collector-base capacitance is further reduced since the entire p-type collector region is fully depleted under normal bias conditions. Pulling the p-well back from the collector edge further lowers collector-substrate capacitance, at the cost of much lower process complexity than would be required for trench isolation. The combination of SCC plus the pwell pullback results in the reduction of

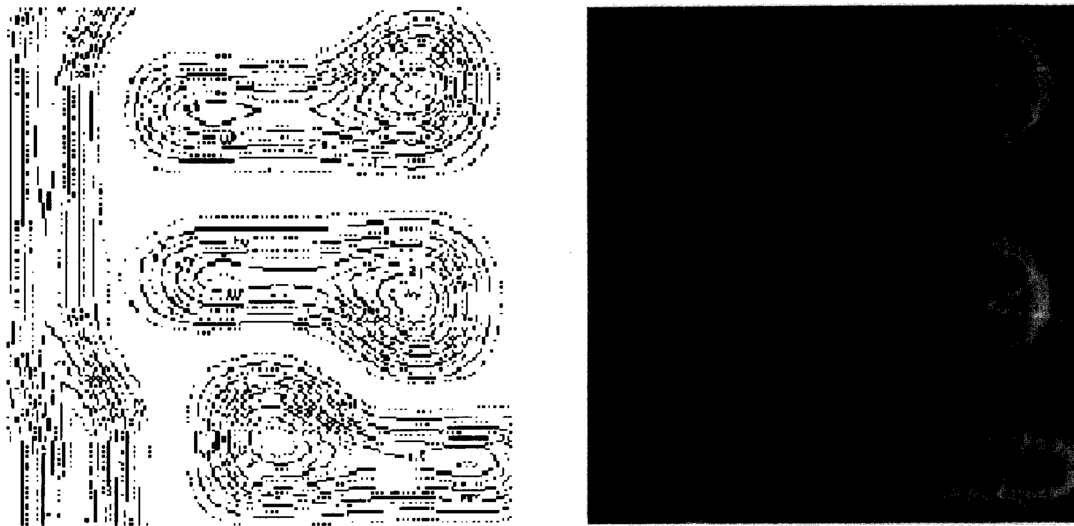


Fig. 16. Comparison of simulation and actual patterning of sub 0.3 μm spaces between latch gates in a 7.32 μm^2 bitcell using Levenson phase shift lithography.

collector-base (C_{CB}) and collector substrate (C_{CS}) capacitances to 5 fF and 8.8 fF (at 0 and 3.0 V, respectively) while maintaining adequate emitter-base (BV_{EBO}), collector-base (BV_{CBO}), and collector-emitter (BV_{CEO}) breakdown voltages of 5.4, 21.0, and 4.6 V, respectively. The power delay product is reduced to 50 fJ, a factor of seven improvement over the previous generation single polysilicon bipolar and a factor of four over a previous generation double polysilicon device [3]. A PNP bipolar transistor has been formed in this process at the cost of a single implant step. Fig. 9 is a schematic cross section of the double polysilicon NPN bipolar transistor, illustrating the SCC region and the p-well pulled back from the collector edge. An SEM cross section of the bipolar with an n-ECL resistor merged into the structure in order to further reduce parasitic capacitances is presented in Fig. 10. Fig. 11 presents Gummel plots for the 0.40 μm NPN and PNP bipolars. Nearly ideal characteristics are achieved down to 10 pA of collector current. Simulated and measured ECL gate delays as a function of switching current are presented in Fig. 12. Merging the ECL resistor into the bipolar structure and employing a walled emitter substantially improve bipolar performance.

E. Thin-Film Transistors

A thin-film PMOS polysilicon transistor (TFT) is required as an SRAM load at the 16 Mb generation in order to improve cell stability and reduce standby current. An undergated TFT structure provides savings in bitcell area relative to an overgated device. Turn-on characteristics for an undergated PMOS TFT with a 150 Å deposited gate dielectric and a 800 Å channel poly are presented in Fig. 13. An on-to-off ratio of 10^5 has been achieved at 3.3 V and 10^6 at 5.0 V. The gate-to-drain offset and gate-to-source underlap have been optimized experimentally. These data are presented in Fig. 14 and 15, respectively. The steep rise in off-current with decreasing gate-to-drain off-set is due to an increase in gate-to-drain electric fields which causes grain-boundary field emission induced leakage current. The sharp drop in on-current with increasing offset is caused by a rise in drain resistance. A comfortable operating range can be found, with sufficient margin against misalignment.

F. Bit-Cell Design

A split word-line bitell architecture has been adopted for the 16 Mb generation [1], [2]. The symmetrical layout improves cell stability over a wider range of process variation and the reduced number of unique feature shapes eases process development. There are now no active fingers, which reduces two-dimensional field oxide encroachment effects [1].

With I-line lithography and manufacturable overlay tolerances, a bitcell area of $2.1 \times 4.1 = 8.61\,\mu m^2$ is achieved. Additionally, the split word-line bitcell layout readily lends itself to implementation of alternating (Levenson) phase shift mask configurations [13] on several critical levels. Optimized phase shift layouts were obtained by means of aerial image simulations using SPLAT [14]. With I-line lithography plus phase shift applied to three polysilicon layers or with deep UV lithography, a bitcell area of $1.9 \times 3.85 = 7.32\,\mu m^2$ can be achieved (Fig. 16).

Four levels of polysilicon and two self-aligned contacts are used in this bitcell to increase packing density. The first self-aligned contact is formed between poly-2 and active and provides a bit-line contact landing pad and V_{SS} pickup. Since this self-aligned contact also forms the bipolar emitter, minimizing the contact resistance (to below $100\Omega \cdot \mu m^2$) is essential. The second self-aligned contact is formed between the first and third poly layers and connects the TFT's and bulk MOSFET's. Because this contact is in series with the TFT, its resistance is less critical and values as great as

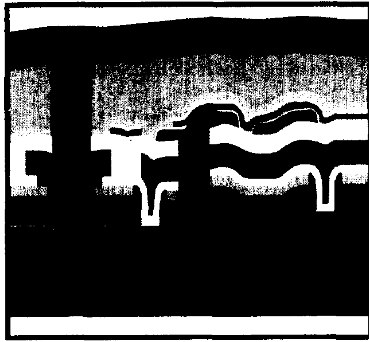


Fig. 17. Schematic cross section of split word-line bitcell, showing four levels of polysilicon, two self-aligned contacts and undergated PMOS TFT.

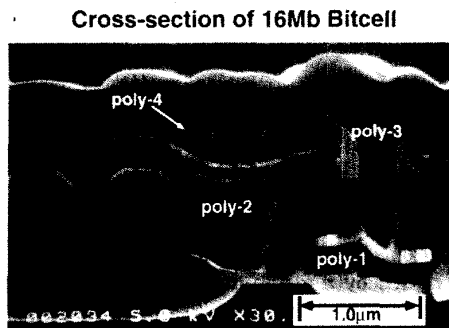


Fig. 18. SEM cross section of split word-line bitcell, showing poly-1 strapped with tungsten polycide, poly-2 strapped with titanium salicide, poly-3 and poly-4 which form an undergated TFT, and the second self-aligned contact.

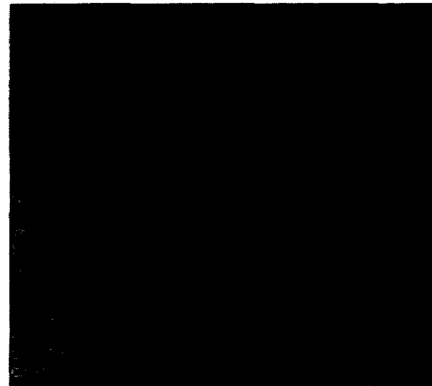


Fig. 19. Top-view SEM photomicrograph of 0.4/0.8 undergated PMOS TFT in the 8.61 μm^2 split wordline bitcell.

10–100 kΩ are acceptable. Fig. 17 is a schematic cross-section of the bitcell showing the four poly layers, two self-aligned contacts, and undergated TFT. Fig. 18 is an SEM cross section of the split word-line bitcell, showing poly-1 strapped with tungsten polycide, poly-2 strapped with titanium salicide, poly-3 and poly-4 which comprise the undergated TFT, and the second self-aligned contact. Fig. 19 is an SEM top-view of the 8.61 μm^2 bitcell illustrating the undergated TFT's.

IV. Conclusions

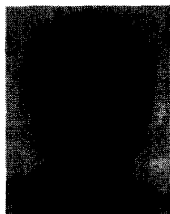
A high-performance quadruple well, quadruple poly BiCMOS process for fast 16 Mb SRAM's has been presented. A split word-line bitcell with an area of 8.61 μm^2 is achieved with conventional I-line lithography and 7.32 μm^2 with I-line plus phase-shift or with deep UV lithography. Isolation and MOSFET designs support active and gate poly pitches of 1.0 and 0.80 μm, respectively. Double polysilicon bipolar transistors with reduced parasitics serve to improve ECL circuit speed.

Acknowledgment

The authors would like to acknowledge the APRDL manufacturing, process engineering, and test groups and would like to thank Wei Wu, Phil Tobin, Fabio Pintchovski, Rick Sivan, and Lou Parrillo for their guidance and support throughout this project. Finally, special thanks are extended to Judy Ko, Lucille Terpollili, Tam Vuong, Keith Lao, Bart James, and Mark Drew for their excellent support.

References

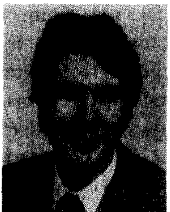
[1] K. Itabashi, K. Mizutani, T. Koga, M. Matumiya, S. Kawashima, M. Sakata, T. Ema, T. Yabu, K. Toyoda, N. Suzuki, and H. Shimada, "A split wordline cell for 16 Mb SRAM using polysilicon sidewall contacts," *IEDM Tech. Dig.*, p. 477, 1991.
[2] H. Ohkubo, S. Horiba, F. Hayashi, T. Andoh, M. Kawaguchi, Y. Ochi, M. Soeda, H. Nozue, H. Miyamoto, M. Ohkawa, T. Shimizu, and I. Sasaki, "16 Mbit SRAM cell technologies for 2.0 V operation," *IEDM Tech. Dig.*, p. 481, 1991.
[3] J. D. Hayden, J. D. Burnett, A. H. Perera, T. C. Mele, F. W. Walczyk, V. Kaushik, C. S. Lage, and Y.-C. See, "Integration of a double-polysilicon emitter-base self-aligned bipolar transistor into a 0.5-μm BiCMOS technology for fast 4-Mb SRAM's," *IEEE Trans. Electron Devices*, vol. 40, p. 1121, 1993.
[4] R. Taft, J. D. Hayden, D. J. Denning, and H. C. Kirsch, "A high-performance low-complexity bipolar technology using selective collector compensation," *IEDM Tech. Dig.*, p. 405, 1992.
[5] J. D. Burnett, C. S. Lage, and A. Bormann, "Soft-error-rate improvement in advanced BiCMOS SRAMs," *Int. Reliab. Physics Symp.*, p. 156, 1993.
[6] C. S. Lage, J. D. Burnett, T. F. McNelly, F. K. Baker, A. Bormann, D. Dreier, and V. Soorholtz, "Soft error rate and stored charge requirements in advanced high-density SRAM's," *IEDM Techn. Dig.*, 1993.
[7] C. Zeller, C. Mazuré, and M. Kerber, "Field-implant-free isolation by double-well split drive-in," *IEEE Electron Device Lett.*, vol. 11, p. 215, 1990.
[8] S. S. Roth, W. J. Ray, C. Mazuré, K. Cooper, H. C. Kirsch, C. D. Gundersion, and Judy Ko, "Characterization of polysilicon encapsulated local oxidation," *IEEE Trans. Electron Devices*, vol. 39, p. 1085, 1992.
[9] S. W. Sun, P. G. Y. Tsui, B. M. Somero, J. Klein, F. Pintchovski, J. R. Yeargain, B. Pappert, and R. Bertran, "A fully complementary BiCMOS technology for sub-half-micrometer microprocessor applications," *IEEE Trans. Electron Devices*, vol. 39, p. 1991, 1992.
[10] T. R. White, W. J. Ciosek, E. J. Prinz, C. F. King, R. Blumenthal, C. W. Stager, B. M. Somero, M. P. Woo, U. Sharma, R. W. Fiordalice, and J. L. Klein, "Extending resist etchback planarization to 0.5 μm logic and ASIC circuits," *1993 SPIE Conf.*
[11] C. Mazuré, C. Gunderson, and B. Roman, "Impact of LDD spacer reduction on MOSFET performance for sub-μm gate/space pitches," *IEDM Tech. Dig.*, p. 893, 1992.
[12] J. D. Hayden, T. C. Mele, A. H. Perera, J. D. Burnett, F. W. Walczyk, C. S. Lage, F. K. Baker, M. P. Woo, W. Paulson, M. Lien, Y.-C. Se, D. Denning, and S. J. Cosentino, "A high-performance 0.5-μm BiCMOS technology for fast 4-Mb SRAM's," *IEEE Trans. Electron Devices*, vol. 39, p. 1669, 1992.
[13] M. D. Levenson, N. S. Viswanathan, and R. A. Simpson, "Improving resolution in photolithography with a phase-shifting mask," *IEEE Trans. Electron Devices*, vol. 29, p. 1828, 1982.
[14] K. K. H. Toh, Memo UCB/ERL M88/30, UC Berkeley, 1988.



James D. Hayden (S'81–M'83–SM'91) received the B.S. degree in engineering physics from the University of Colorado, and the M.S.E.E. degree from the University of Arizona.

From 1981 to 1983 he worked as an RF Test Engineer at Bell Aerospace. In 1983 he joined Advanced Micro Devices as a Modeling Engineer, developing circuit simulation models for EPROM and EEPROM products. During 1985–1986 he worked at NCR Microelectronics in Colorado Springs, CO, with device design responsibilities in the development of a 1 μm CMOS process. In 1987 he joined INMOS Corporation as a Device Physicist, working on the development of 1.2 and 0.8 μm SRAM processes. Since 1988 he has been with Motorola's Advanced Products Research and Development Laboratories, where he has been working on bipolar and MOS device design and SRAM bit cell development of 0.50 μm and 0.35 μm BiCMOS processes. He is now Section Manager for 0.25 μm BiCMOS SRAM technology development. He has authored or coauthored over 40 papers and holds 25 US patents.

He is a Member of the Technical Staff and received a Distinguished Innovator award at Motorola.



Robert C. Taft was born in Vienna, Austria. He received the the B.Sc. degree (honors) in mathematics and physics from the University of Victoria, Canada, in 1985. He received the M.S. and Ph.D. degrees in electrical engineering from Stanford University. His dissertation focused on the Ge_xSi_{1-x}/Si inversion-base transistor or BICFET structure.

In 1990 he joined the APRDL division of Motorola and designed the selectively compensated collector (SCC) bipolar transistor for Motorola's 0.35 μm BiCMOS SRAM technology. His responsibilities later included the 0.35 μm BiCMOS pilot baseline and to assist the SRAM Memory Design group. In 1994 he joined East Coast Labs, a start-up fabless semiconductor company.

P. Kenkare, for a photograph and biography, see *IEEE Transactions on Electron Devices*, vol. 41, p. 56, Jan. 1994.

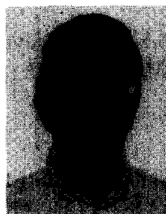
C. Mazuré, photograph and biography not available at time of publication.

C. Gunderson, for a photograph and biography, see *IEEE Transactions on Electron Devices*, vol. 41, p. 56, Jan. 1994.

B.-Y. Nguyen, for a photograph and biography, see *IEEE Transactions on Electron Devices*, vol. 41, p. 56, Jan. 1994.

M. P. Woo, for a photograph and biography, see *IEEE Transactions on Electron Devices*, vol. 39, p. 1669, July 1992.

C. Lage, for a photograph and biography, see *IEEE Transactions on Electron Devices*, vol. 39, p. 1669, July 1992.



Bernard J. Roman received the Ph.D. in solid state physics from Northwestern University in 1969.

He began his career working on micromagnetic and compound semiconductor device technology at AT&T Bell Labs. He is now the Deep UV Lithography Technology Group Leader at Motorola's Advanced Products Research and Development Group, where his responsibilities include definition of DUV tooling and processes as well as transfer to manufacturing.

Dr. Roman is a member of APS and SPIE.

S. Radhadrishna, photograph and biography not available at time of publication.

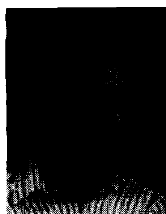
R. Subrahmanyan, photograph and biography not available at time of publication.

A. R. Sitaram received the B.E. in metallurgy from KREC Suratkal in 1985, and the M.S. and Ph.D. in material science from Rensselaer Polytechnic Institute in 1988 and 1990, respectively.

He has worked at the Advanced Products R&D Laboratory of Motorola, Inc., in Austin, TX, since 1990. His research interests are in the areas of silicides, metal CVD, and rapid thermal processing.

P. Pelley, photograph and biography not available at time of publication.

J.-H. Lin, photograph and biography not available at time of publication.



Kevin Kemp was born in South Africa. He received the B.Sc. and M.Sc. degree in electrical engineering from the University of Natal, Durban, South Africa, in 1981 and 1985, respectively. He received the Ph.D. in electrical engineering from Clemson University, South Carolina, in 1989.

From 1985 to 1987 he worked at the National Electrical Engineering Research Institute of the Council for Scientific and Industrial Research in Pretoria, South Africa. In 1989 he joined the Advanced Products Research and Development Laboratory at Motorola in Austin, TX. He is currently involved in the development of advanced i-line and DUV lithography for sub-0.5 μm applications.

H. Kirsch, for a photograph and biography, see *IEEE Transactions on Electron Devices*, vol. 41, p. 56, Jan. 1994.