Integration of a Double-Polysilicon Emitter–Base Self-Aligned Bipolar Transistor into a 0.5-μm BiCMOS Technology for Fast 4-Mb SRAM's

James D. Hayden, *Senior Member, IEEE*, J. David Burnett, Asanga H. Perera, *Member, IEEE*, Thomas C. Mele, *Member, IEEE*, Fred W. Walczyk, Vidya Kaushik, Craig S. Lage, and Yee-Chaung See, *Senior Member, IEEE*

***Abstract*—The single-polysilicon non-self-aligned bipolar transistor in a 0.5-μm BiCMOS technology has been converted into a double-polysilicon emitter–base self-aligned bipolar transistor with little increase in process complexity. Improved bipolar performance in the form of smaller base resistance and base–collector capacitance, larger knee current, higher peak cutoff frequency, and shorter ECL gate delay has been demonstrated. This technology will prove useful in meeting the requirements for higher performance in fast, high-density, SRAM circuits.**

I. Introduction

BICMOS has become accepted as the process of choice for fast, high-density, SRAM circuits [1]–[3]. As circuit speeds continue to increase, ECL circuit design techniques will be more extensively employed because of the potential for reduction in gate delay. ECL type circuitry places a demand on lower bipolar parasitics and correspondingly improved bipolar performance. In particular, a double-polysilicon emitter–base or "fully" self-aligned (FSA) bipolar transistor offers reduced collector–base capacitance and base resistance and improved ECL gate delay when compared to a single polysilicon, non-self-aligned device (NSA).

Fast, high-density SRAM circuits place a premium on both packing density and circuit performance. At the 4-Mb density level a bit-cell size of less than 20 μm^2 is required in order to meet both packing density and package size constraints. This requirement is met by the use of a 0.5-μm generation CMOS technology and by the introduction of a self-aligned contact landing pad structure [2], [3]. Fast static RAM's (FSRAM's) at the 4-Mb level must have access times in the range of 15 ns or better. This requirement is achieved by adding a medium performance, single-polysilicon, non-self-aligned bipolar transistor to the already existing 0.5-μm CMOS technology [3].

In many 4-Mb generation SRAM technologies, an additional polysilicon layer is introduced in order to form self-aligned contact landing pads and local interconnect. These together allow the bit-cell area to be reduced to below 20 μm^2 [2], [3]. In the self-aligned contact landing pad structure, the second polysilicon layer makes contact with single-crystal silicon between a pair of first polysilicon word lines. In particular, the bit-line contacts "land" on a pad formed of second polysilicon. This pad, in turn, sits between a pair of poly-1 word-lines. In this fashion, the space between bit-line contact and poly-1 word-line can be reduced, as well as the active enclosure of bit-line contact and the bit-cell area is thus decreased. Fig. 1(a) and (c) demonstrates the potential increase in packing density that can be achieved by introducing the self-aligned contact landing pad structure.

In the present work, the self-aligned landing pad structure has been used to convert the single-polysilicon emitter–base non-self-aligned bipolar in an existing 0.50-μm BiCMOS technology [3] into a double-polysilicon emitter–base self-aligned bipolar transistor with little increase in process complexity. Fig. 1(b) and (d) compares the NSA and FSA bipolar transistor structures. In the FSA device the first polysilicon layer forms the extrinsic base contact, while the second polysilicon layer forms the polysilicon emitter. In converting from the landing pad structure, the gate oxide must be removed from beneath the first polysilicon layer. This can be accomplished during buried contact processing which is already present in the process. The polysilicon forming the extrinsic base contact must also be doped p^+, which requires the addition of a photoresist patterning and an ion-implantation step. The polysilicon emitter is doped by arsenic implantation, which is already the case for the NSA bipolar transistor and the contact landing pad. The double-polysilicon bipolar can thus be formed from the contact landing pad

Manuscript received June 26, 1992; revised December 10, 1992. The review of this paper was arranged by Associate Editor K. Shenai.

J. D. Hayden, J. D. Burnett, A. H. Perera, T. C. Mele, F. W. Walczyk, V. Kaushik, and C. S. Lage are with Advanced Products Research and Development Laboratory, Motorola Inc., Austin, TX 78721.

Y. C. See is with Advanced Custom Technology Center, Motorola Inc., Mesa, AZ 85210.

IEEE Log Number 9208556.

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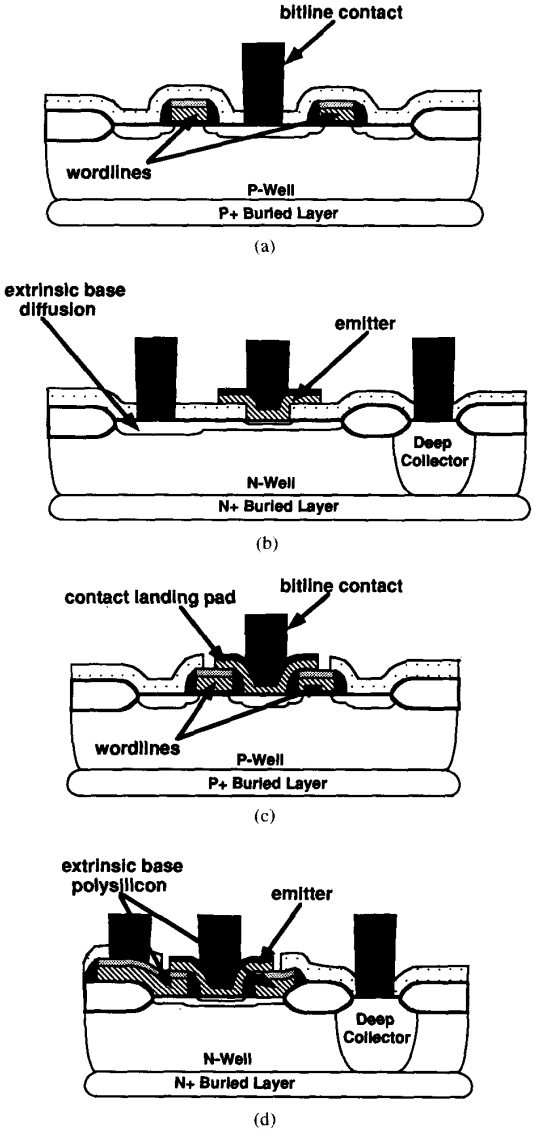


Fig. 1. (a) Schematic cross section of non-self-aligned bit-line contact landing pad demonstrating the large spacing required between polysilicon word-lines and bit-lines contacts. (b) Schematic cross section of single-polysilicon non-self-aligned n-p-n bipolar transistor in existing 0.5-μm BiCMOS techology. (c) Schematic cross section of self-aligned bit-line contact landing pad. (d) Schematic cross section of double-polysilicon emitter-base self-aligned bipolar transistor developed in this paper.

structure by the addition of only a single patterning and implantation step.

II. Process

The starting point for this work is a 0.5-μm BiCMOS technology for fast 4-Mb SRAM circuits which employs a single-polysilicon NSA bipolar transistor [3]. This CMOS-based BiCMOS process assumes a 5-V power supply. In this process, bipolar performance has been traded off in a number of cases for reduced process complexity and improved manufacturability. Fabricating a yielding 4-Mb SRAM circuit may not allow use of some of the complicated process technology required for a super high-performance bipolar transistor. A reduction in process steps is achieved at the expense of a relatively high collector substrate capacitance C_{CS}, by using self-aligned complementary buried layers and twin wells. An n^+ buried layer plus a deep collector implant serve to lower collector resistance for BiCMOS applications. p^+ buried layers are required for isolation between n^+ buried layers. The same n-well doping is found to give acceptable bipolar collector-emitter breakdown BV_{CEO} and PMOS punchthrough resistance. This process employs a nominal grown epitaxial thickness of 1.6 μm, for a final flat zone width of 0.4 μm.

This technology uses a LOCOS-based isolation, FMPBL or Framed-Mask Poly Buffered LOCOS [4], rather than trench in order to reduce process complexity. Again, bipolar performance has been sacrificed for manufacturability. FMPBL [4] achieves an active pitch of 1.3 μm, consistent with the requirements of a 4-Mb SRAM bit-cell. Narrow-width effects are reduced down to an effective channel width of 0.25 μm.

Surface-channel NMOS and buried-channel PMOS transistors are fabricated with a 150-Å gate oxide thickness. These transistors display good MOSFET characteristics to minimum effective channel lengths of 0.35 and 0.50 μm, respectively. Off leakage is held to below 1 pA/μm of channel width. CMOS device characteristics have been reported on elsewhere [3]. Both n-channel and p-channel transistors incorporate moderately doped drain (MDD) extensions to increase their resistance to short-channel effects and hot-carrier degradation. A variety of MDD spacer schemes are available in this process, including reverse sequence, disposable polysilicon spacers [5], and permanent dielectric spacers comprised of silicon nitride or TEOS (tetra-ethyl-orthyl silane).

The process features three layers of polysilicon: the first is used to form the MOSFET gates; the second the bipolar emitter, a self-aligned contact landing pad and a global interconnect; and the third a teraohm load resistor in the bit-cell. The second polysilicon layer is optionally strapped with titanium salicide or tungsten polycide. As described previously, the self-aligned landing pad is formed by allowing the second polysilicon to contact single-crystal silicon between a pair of poly-1 word-lines. Dielectric spacers, as well as a dielectric cap on top of the first polysilicon layer provide isolation between poly-1 and poly-2. It was found that using this landing pad for the bit-line contact in the memory array provides a significant reduction in bit-cell area while degrading the drive current in the pass transistor by only a few percent.

The original process featured a single-polysilicon NSA vertical n-p-n bipolar transistor, where the second poly layer is used for the emitter. The extrinsic base is formed with an implant into single-crystal silicon. This implant is offset lithographically from and, hence, not self-aligned

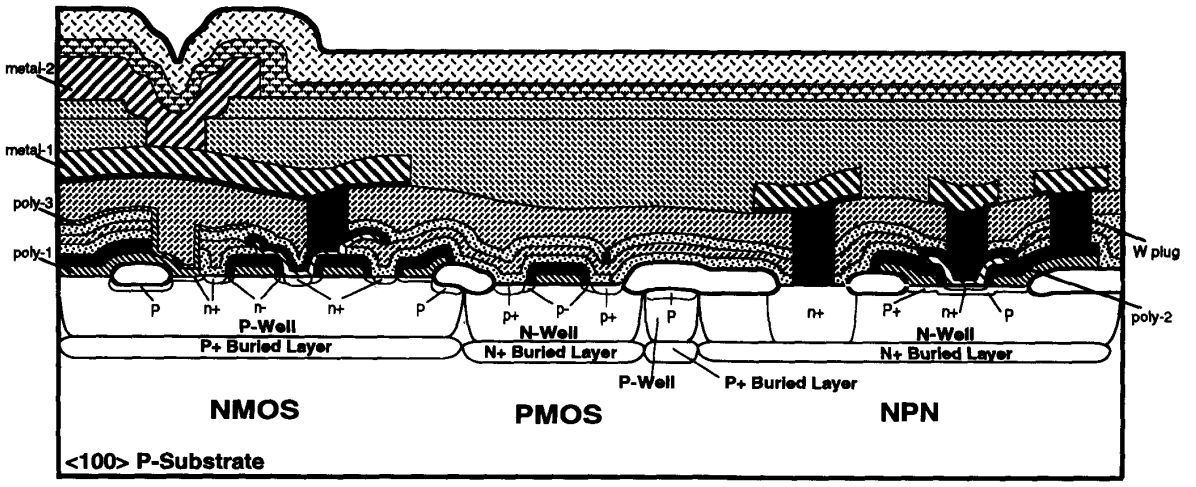


Fig. 2. Schematic cross section of the 0.5-μm BiCMOS technology showing the double-polysilicon emitter-base self-aligned bipolar transistor; NMOS transistor with self-aligned contact landing pad; and PMOS transistor. Three layers of polysilicon and two layers of metallization are also displayed.

to the emitter. A rapid thermal anneal step serves to break up the interfacial oxide between emitter poly and single-crystal silicon, activate the emitter dopant, and drive arsenic from the poly emitter into single-crystal silicon, as well as to provide planarization prior to deposition of the first metal layer. Two levels of metallization are provided in this technology.

In this work, the single-polysilicon NSA bipolar transistor was converted to a double-polysilicon FSA structure by using the first polysilicon layer to form the extrinsic base contact. In this configuration, the extrinsic base now completely surrounds the emitter. The second polysilicon continues to be used for the emitter. The emitter and extrinsic base are separated by a dielectric spacer, and are thus self-aligned. The base resistance R_B and collector–base capacitance C_{CB} can be then reduced relative to the NSA transistor where emitter and extrinsic base are offset lithographically. The final dielectric spacer consists of the MOSFET MDD spacer as well as the TEOS interpoly dielectric remaining after the etch of the emitter opening. Formation of the FSA bipolar is thus identical to that of the self-aligned contact landing pad except that the gate oxide is removed from the bipolar area prior to deposition of the first polysilicon layer, the extrinsic base poly is doped p-type, and the source/drain implants are blocked from the emitter area. As discussed above, this requires only the addition of a single poly doping mask in the process, a minor increase in process complexity. The optimization of the FSA bipolar transistor and the landing pad can be performed simultaneously. Interfacial oxide and dopant loss during polycide formation are found to affect both structures similarly. The emitter resistance in the FSA bipolar and the poly-2 to silicon contact resistance in the landing pad structure are found to track one another quite closely across a wide range of emitter formation conditions [6]. Because conversion of the bipolar from a single-polysilicon NSA device to a double-polysilicon FSA involves only minor perturbations to the original process flow, no significant changes in MOSFET devices characteristics are observed.

Fig. 2 is a schematic cross section of the technology depicting the double-polysilicon bipolar transistor as well as an NMOS transistor with a self-aligned polysilicon contact landing pad connecting to its drain and a PMOS transistor. All three polysilicon levels, MOSFET gate and bipolar extrinsic base, bipolar emitter and self-aligned landing pad, and SRAM load resistor can be seen. Contacts and vias plus two levels of metallization are also present.

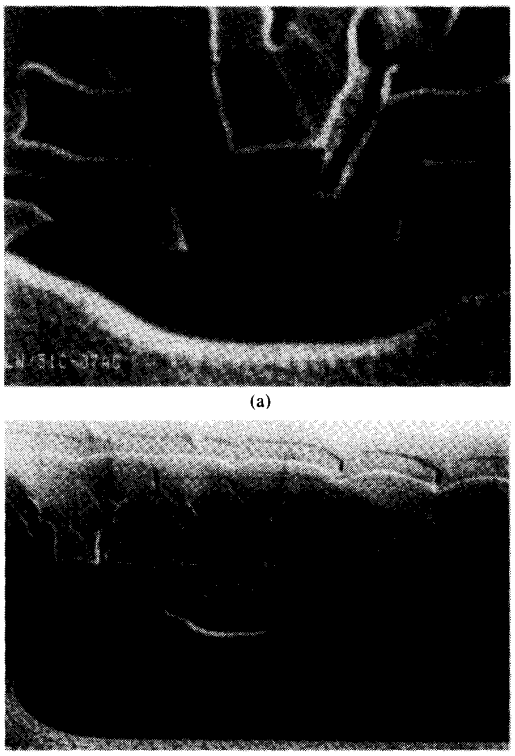
The extrinsic base region was experimentally optimized by varying the extrinsic base implant dose while maintaining the remainder of the process unchanged. Base resistance was minimized while ensuring an adequate base–emitter breakdown voltage. The effect of varying the epitaxial layer thickness and of leaving out the p^+ buried layer were also investigated in this work. FSA and NSA transistors were fabricated on the same wafers, providing for excellent comparisons.

III. Experimental Results and Discussion

A. DC Characteristics

Excellent bipolar characteristics have been obtained for double-polysilicon FSA transistors with physical emitter widths as small as 0.4 μm. Figs. 3 and 4 are SEM and TEM cross sections, respectively, of an FSA bipolar with a 0.8 $\times$ 2.4 μm emitter. In this case, permanent nitride spacers have been used during MDD formation. The secondary dielectric spacer formed during etch of the emitter opening is also evident in the TEM. Fig. 5 presents SIMS doping profiles of the emitter arsenic and active base boron concentrations. The nominal emitter depth and base width are ι100 and 1300 Å, respectively.

Gummel characteristics for an FSA device with a pat-



(a)

(b)

Fig. 3. (a) SEM cross section of double-polysilicon emitter–base self-aligned bipolar transistor with a 0.8 × 2.4 μm emitter. (b) SEM cross section of double-polysilicon emitter–base self-aligned bipolar transistor with a 0.8 × 2.4 μm emitter.

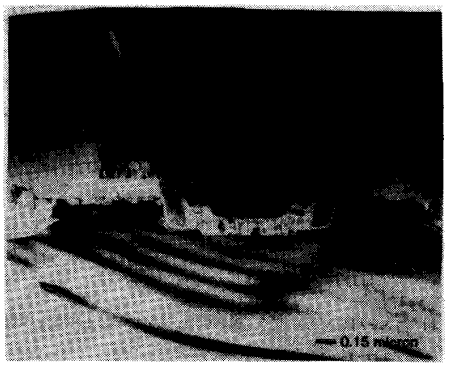


Fig. 4. TEM cross section of double-polysilicon emitter–base self-aligned bipolar transistor with a 0.8 × 2.4 μm emitter.

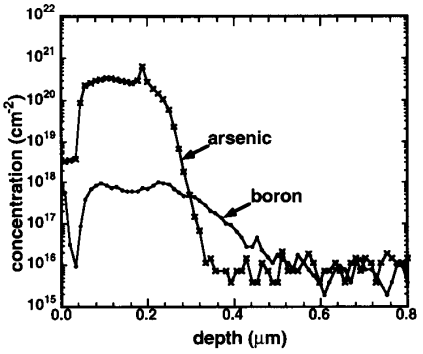


Fig. 5. SIMS profiles for double-polysilicon emitter–base self-aligned bipolar transistor.

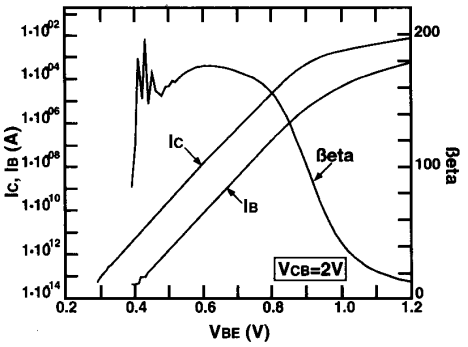


Fig. 6. Gummel plot of double-polysilicon emitter–base self-aligned bipolar transistor with a 0.4 × 1.2 μm emitter.

terned emitter dimension of 0.4 × 1.2 μm exhibit ideal bipolar characteristics to below 0.1 pA/μm^2 as shown in Fig. 6. The current gain is essentially constant over 6–7 orders of magnitude. Some evidence of the reverse Early effect is apparent. Arrays of 1000 FSA transistors do not exhibit an increased incidence of shorts relative to comparable arrays of NSA transistors. This indicates no significant etch damage during extrinsic base formation.

Fig. 7 compares Gummel plots and Table I presents transistor parameters for FSA double-polysilicon and NSA single-polysilicon bipolar transistors fabricated on the same wafer. The FSA transistor exhibits higher base current and lower collector current at intermediate emitter–base voltages. Lateral encroachment of the extrinsic base reduces the emitter efficiency at the emitter edge as well as decreasing the effective emitter area. The FSA transistor displays lower base resistance at high current levels and some evidence of forward excess tunneling [7] at very low currents for the highest extrinsic base implant doses. This is seen in Fig. 8 where an increase in nonideal base current component is apparent.

The FSA transistor provides an improvement in base resistance R_B over the NSA device because of the reduced spacing between emitter and extrinsic base regions. This improvement comes, however, at the expense of some degradation in emitter–base breakdown voltage BV_{EBO}. Fig. 9 illustrates that base resistance can be traded off against emitter–base breakdown voltage by varying the extrinsic base implant dose. Additional process modifications, in the form of reduced back-end heat and wider dielectric spacers would further improve this tradeoff. Much of the reduction in R_B is due to the double-base configuration. Fig. 10 compares results from NSA single- and double-base transistors with FSA transistors where

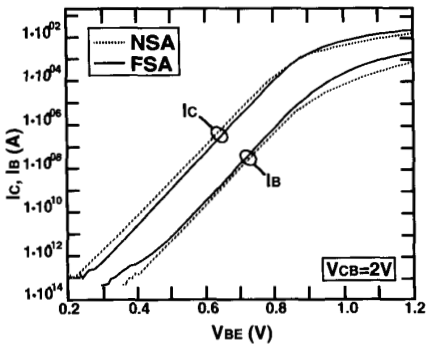


Fig. 7. Gummel plots for double-polysilicon emitter–base self-aligned (FSA) and single-polysilicon non-self-aligned (NSA) bipolar transistors with 0.8 × 2.4 μm emitters.

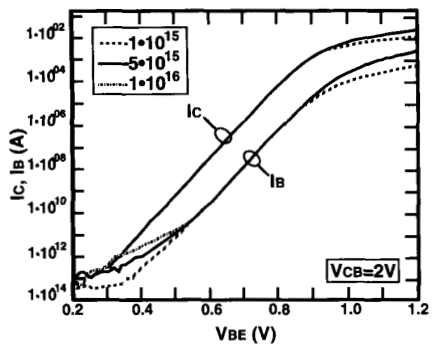


Fig. 8. Gummel plots for double-polysilicon emitter–base self-aligned bipolar transistors with 0.8 × 2.4 μm emitters. The extrinsic base dose has been varied from 2×10^{15} to 1×10^{16} cm^{-2}.

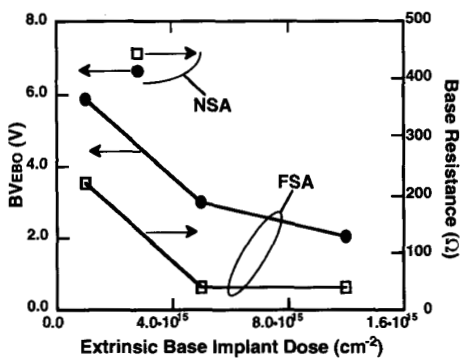


Fig. 9. Base–emitter breakdown voltage and base resistance as a function of extrinsic base implant dose for bipolar transistors with 0.8 × 2.4 μm emitters.

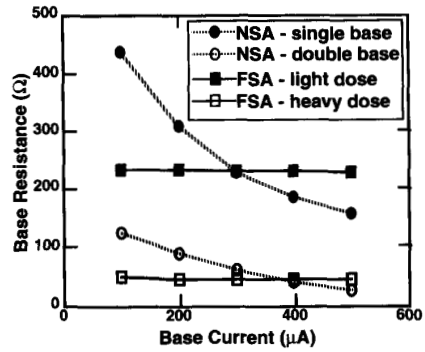


Fig. 10. Base resistance as a function of base current for single-polysilicon bipolar transistors and for double-polysilicon bipolars with light and heavy extrinsic base doses of 2×10^{15} and 1×10^{16} cm^{-2}, respectively. The emitter area is 0.8 × 2.4 μm.

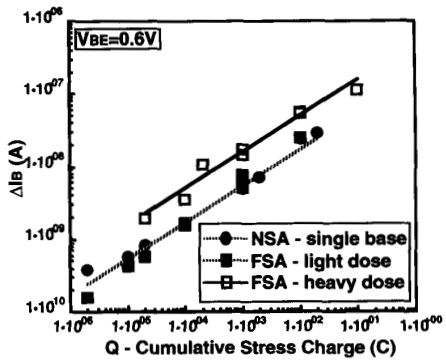


Fig. 11. The result of hot-carrier stress on bipolar characteristics for single-polysilicon bipolar transistors and for double-polysilicon bipolars with light and heavy extrinsic base doses. Increase in the nonideal base current component as a function of cumulative stress charge during emitter–base reverse bias stress. The emitter area is 0.8 × 2.4 μm.

TABLE I
n-p-n TRANSISTOR PARAMETERS
(emitter area = 0.8 × 2.4 μm^2)

Parameter	Units	NSA	FSA
BV_{CBO}	(V)	18	18
BV_{CEO}	(V)	6.5	6.5
C_{EB}	(fF)	8	8
C_{CB}	(fF)	13	8
C_{CS}	(fF)	48	41
R_E	(Ω)	13	12

the extrinsic base wraps around the entire emitter region. The FSA structure simultaneously reduces R_B and device area, which in turn decreases collector–base capacitance C_{CB}. The roll-off of base resistance with increasing base current is diminished with the FSA structure because lateral encroachment of the extrinsic base dopant inhibits charge modulation of the intrinsic base around the periphery of the emitter.

The effect of hot-carrier stressing on bipolar characteristics is studied in Fig. 11 for FSA and NSA transistors. At low extrinsic base implant doses, there is little difference between the FSA and NSA devices. Higher extrinsic base doses result in a more rapid increase in the nonideal base current component ΔI_B under reverse-bias emitter–base stress. The higher doping around the periphery of the emitter–base junction results in increased electric fields during emitter–base avalanche breakdown and a more rapid generation of interface states in the oxide overlying the junction edge.

The wrap-around base contact in the FSA transistor produces a more uniform electron injection around the

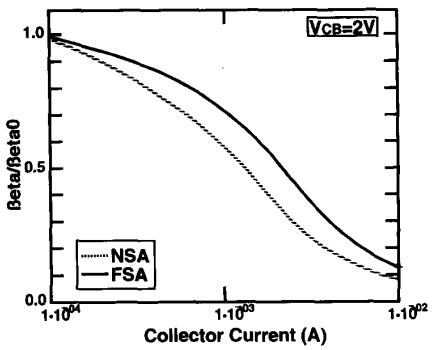


Fig. 12. Normalized transistor gain as a function of collector current for double-polysilicon emitter–base self-aligned and single-polysilicon non-self-aligned bipolar transistors with 0.8 × 2.4 μm emitters.

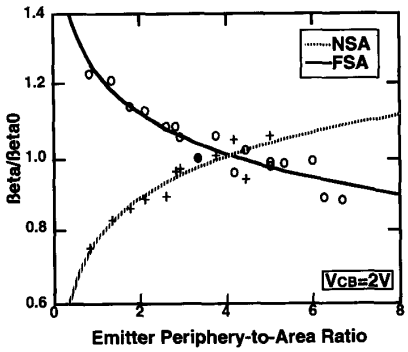


Fig. 13. Normalized transistor gain as a function of emitter periphery-to-area ratio for double-polysilicon emitter–base self-aligned and single-polysilicon non-self-aligned bipolar transistors with 0.8 × 2.4 μm emitters.

emitter edge when compared to a single-base NSA bipolar. By reducing current crowding at the emitter edge, the onset of the Kirk effect or base push-out is delayed and a higher knee current results [8], as shown in Fig. 12.

The geometry dependence of transistor current gain manifests itself differently between FSA and NSA transistors. This is demonstrated in Fig. 13. The collector current density increases with smaller periphery-to-area ratio for both type devices. Diffusion of emitter arsenic into single-crystal silicon increases the effective area for electron injection. For NSA transistors, the base current density is relatively constant and the current gain or beta increases. The base current is dominated by hole recombination at the emitter polysilicon/silicon interface and thus scales with patterned emitter area. For FSA transistors, encroachment of the extrinsic base dopant causes the base current density to increase more rapidly than collector current, forcing beta to decrease. Lateral encroachment of boron from the extrinsic base poly pinches the corners of the emitter, decreasing the emitter Gummel number and increasing hole injection at the emitter edge.

B. AC Characteristics

The base transit time is not expected to vary significantly between FSA and NSA transistors on the same wafer. Fig. 14 shows that the peak cutoff frequency f_T, on the other hand, is higher for the FSA device. This is due to a delay in the onset of base pushout and a reduction in parasitic capacitances (C_{CB}), compensating for any narrow emitter effects [9]. Higher cutoff frequencies could be obtained with a selectively implanted collector (SIC) [10] and/or a double-diffused emitter–base [11] approach.

The FSA structure provides a significant improvement in ECL gate delay relative to the NSA transistor, as illustrated in Fig. 15. The reduction in collector–base capacitance and base resistance are responsible for the improvement. Converting from an NSA to an FSA bipolar reduces ECL gate delay from 140 to 70 ps/gate and 110 to 60 ps/gate for conservative and aggressive layout rules, respectively. Here, conservative is defined as design rules

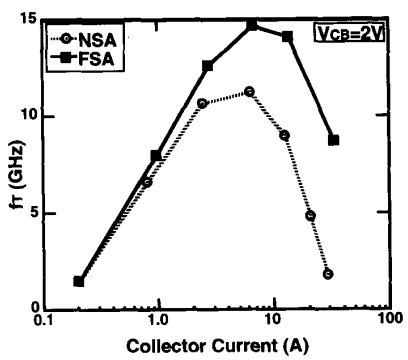


Fig. 14. Cutoff frequency as a function of collector current density for double-polysilicon emitter–base self-aligned and single-polysilicon non-self-aligned bipolar transistors with 0.8 × 20 μm emitters.

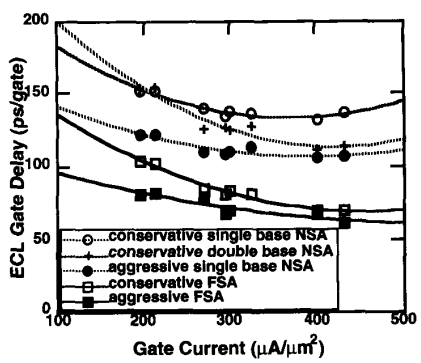


Fig. 15. ECL gate delay as a function of gate current for double-polysilicon emitter–base self-aligned and single-polysilicon non-self-aligned bipolar transistors with conservative and aggressive layout design rules. The double-polysilicon transistor had an extrinsic base implant dose of 2×10^{15} cm^{-2}.

consistent with processes presently in production while aggressive refers to processes expected to be transferred to production in the next few years. Loaded BiCMOS gate delay is also reduced 10–20% with the FSA structure, again because of the reductions in R_B and C_{CB}. ECL gate

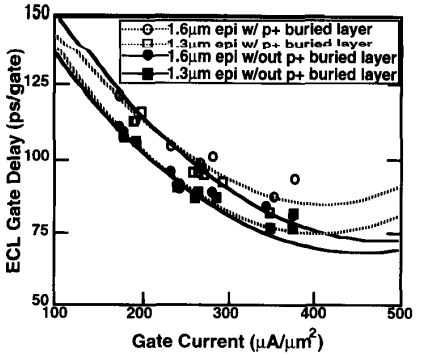


Fig. 16. ECL gate delay as a function of gate current for double-polysilicon emitter-base self-aligned bipolar transistors with 1.3- versus 1.6-μm as-grown epitaxial layer thickness and with and without p^+ buried layer. The double-polysilicon transistor had an extrinsic base implant dose of 2×10^{15} cm^{-2}.

delay can be further improved by eliminating the p^+ buried layer which decreases collector–substrate capacitance C_{CS}, and by reducing the epitaxial layer thickness, which increases the knee current and lowers the collector resistance. These trends are illustrated in Fig. 16.

IV. Conclusions

A double-polysilicon fully-self-aligned bipolar transistor has been successfully substituted for a single-polysilicon non-self-aligned bipolar transistor in a 0.5-μm BiCMOS technology with little increase in process complexity. Greatly improved bipolar performance has been demonstrated.

Acknowledgment

The authors wish to thank H. Kirsch, R. Sivan, and L. Parrillo for their support and guidance throughout this project. Additionally, the authors would like to thank the APRDL manufacturing, process, and test engineering groups.

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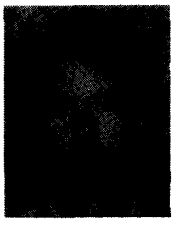
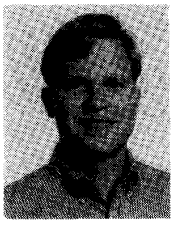


James D. Hayden (S'81-M'83-SM'91) received the B.S. degree in engineering physics from the University of Colorado, Boulder, and the M.S.E.E. degree from the University of Arizona, Tucson.

He worked as an RF Test Engineer at Bell Aerospace from 1981 to 1983. In 1983 he joined Advanced Micro Devices as a Modeling Engineer, developing circuit simulation models for EPROM and EEPROM products. From 1985 to 1986 he worked at NCR Microelectronics in Colorado Springs, CO, with device design responsibilities in the development of a 1 μm CMOS process. In 1987 he joined INMOS Corporation as a Device Physicist, working on the development of 1.2- and 0.8-μm SRAM processes. Since May 1988 he has been with Motorola's Advanced Products Research and Development Laboratories, Austin, TX. His duties have included bipolar and MOS device design and SRAM bit cell development for 0.50- and 0.35-μm BiCMOS processes.

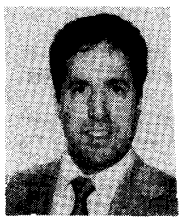


J. David Burnett was born in Slaton, TX, in 1961. He received the B.S.E.E. degree from Texas A&M University, College Station in 1984 (summa cum laude), and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 1986 and 1990. His dissertation focused on the reliability of bipolar devices.

In 1990, he joined the Advanced Products Research and Development Laboratory of Motorola in Austin, TX, working on 0.5-μm BiCMOS technology for SRAM's. He was selected as a receipient of the 1991 SRC Technical Excellence Award.

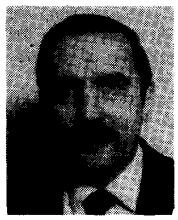
Asanga H. Perera (S'87-M'89-S'90-M'90) received the B.Sc. degree in electrical engineering from Manhattan College, Riverdale, NY, in 1984. In 1987 and 1990 he obtained the M.Sc. and Ph.D. degrees in electrical engineering, respectively, from Cornell University, Ithaca, NY.

His work at the National Nanofabrication Facility at Cornell investigated the impact of MOSFET series resistance on continued device scaling into the sub-0.25-μm domain. In 1990, he joined the Advanced Products Research and Development Laboratory at Motorola Inc., in Austin, TX, where he worked on developing a 0.5-μm BiCMOS technology used for 4M SRAM products. His current research interests are silicides, advanced isolation, and device scaling.



Thomas C. Mele (S'83–M'88) was born in Ann Arbor, MI, on March 31, 1961. He received the B.S. degree (magna cum laude) in electrical engineering from the University of Delaware, Newark, in 1983. He performed his doctoral studies at Cornell University, Ithaca, NY, and received the Ph.D. degree in electrical engineering in 1988.

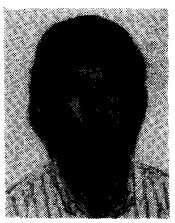
In 1988, he joined Motorola, Inc., Austin, TX, as a member of the Advanced Products Research and Development Laboratory. He spent three years as a device engineer involved in process integration for 0.5-μm CMOS and BiCMOS fast SRAM's. Since 1990 he has been the Section Manager of the APRDL Diffusion/Epi Process Engineering Group.



Fred W. Walczyk was born in Fall River, MA, in 1947. He received the B.S. degree from the University of Massachusetts at Dartmouth in 1969 and the M.S. degree from Bowling Green State University in 1979, both in physics.

In 1969 he joined Texas Instruments to do development for radiation tolerant bipolar and J-FET devices. In 1980 he joined Digital Equipment Corporation where he engaged in CMOS and BiCMOS process development and integration for custom microprocessors. Since 1984 he has been with Motorola Inc., Austin, TX, working on advanced CMOS and BiCMOS process integration and device engineering projects including nonvolatile and SRAM memory development.

Vidya Kaushik, photograph and biography not available at the time of publication.



Craig Lage received the B.S. degree in physics from the California Institute of Technology, Pasadena, in 1976, and the M.S. degrees in nuclear engineering and electrical engineering from the University of Wisconsin at Madison in 1978 and 1979.

He was employed at Hewlett-Packard in Corvallis, OR, from 1979 until 1985, doing process integration work on CMOS technologies. In 1985 he joined Fairchild Semiconductor in Puyallup, WA (subsequently acquired by National Semiconductor), here he and his coworkers developed technology used for high-speed BiCMOS 256 K and 1-Mb SRAM's. Since 1990 he has been with Motorola's Advanced Products Research and Development Laboratory in Austin, TX, working on high-speed BiCMOS SRAM technology.

Yee-Chaung See (S'75–M'80–SM'90) received the B.S. degree in physics from National Taiwan Univerity, Hsinchu, in 1971, the M.S. degrees in physics and electrical engineering from Carnegie-Mellon University, Pittsburgh, PA, in 1975, and the Ph.D. degree in electrical engineering from University of Pittsburgh in 1980.

From 1980 to 1983, he was a member of the technical staff at the Semiconductor Process and Design Center, Texas Instruments, Inc. His development efforts involved advanced CMOS technology, plasma etch and $TiSi_2$ silicide. In 1983, he joined Motorola Inc. in Austin, TX. He was a device engineering manager in MOS8, responsible for the start-up of the 2- and 1.5-μm products, the transfer of the 1.2-μm EPROM and SRAM processes, and the establishment of the CMOS product transfer methodology. In 1987 he joined the Advanced Products Research and Development Laboratory as a manager of advanced development involved with the joint development with Toshiba Corp. From 1988 to 1989, he was responsible for the successful technology development and fabrication of the 0.5-μm "Superchip" for the VHSIC Phase-II program. Since mid-1989, he has been managing the 0.5-μm BiCMOS technology development for the high-speed SRAM applications. In October 1990, he moved to the Advanced Technology Center in Mesa, AZ, where he is a manager of advanced development responsible for sub-0.5-μm BiCMOS and SiGe technology. Currently he is a senior member of the technical staff.