A High-Performance 0.5-μm BiCMOS Technology for Fast 4-Mb SRAM's

James D. Hayden, *Senior Member, IEEE,* Thomas C. Mele, *Member, IEEE,* Asanga H. Perera, David Burnett, Fred W. Walczyk, Craig S. Lage, Frank K. Baker, Michael Woo, Wayne Paulson, Mitch Lien, Yee-Chaung See, *Senior Member, IEEE,* Dean Denning, and Stephen J. Cosentino, *Member, IEEE*

***Abstract*—A high-performance 0.5-μm BiCMOS technology has been developed for a fast 4-Mb SRAM class of circuits. Three layers of polysilicon are used to achieve a compact four transistor SRAM bit cell size of less than 20 μm^2 by creating self-aligned bit-sense and V_{ss} contacts. A WSi_x polycide emitter n-p-n transistor with an emitter area of 0.8 × 2.4 μm^2 provides a peak cutoff frequency (f_T) of 14 GHz with a collector–emitter breakdown voltage (BV_{CEO}) of 6.5 V. A selectively ion-implanted collector (SIC) is used to compensate the base channeling tail in order to increase f_T and knee current without significantly affecting collector–substrate capacitance. ECL gate delays as fast as 105 ps are obtained with this process.**

I. Introduction

A 0.5-μm BiCMOS technology designed to support a high-performance fast 4-Mb SRAM class of products must satisfy a number of requirements. The SRAM bitcell area must be less than 20 μm^2 to meet package size constraints. The active transistors, and particularly the gate oxide thickness, must be designed to support a 5-V power supply. The NMOS and PMOS transistors should exhibit acceptable MOSFET behavior for minimum effective channel lengths of 0.35 and 0.50 μm, respectively. To maintain the performance advantage of bipolar over CMOS, the n-p-n transistor should have a peak cutoff frequency f_T exceeding 10 GHz while the bipolar snapback voltage BV_{CEO} is maintained above 6.5 V. To satisfy all of these requirements, a 0.5-μm BiCMOS technology has been developed that combines a triple polysilicon process architecture with Framed Mask Poly-Buffered LOCOS (FMPBL) isolation [1], a disposable poly spacer module, a polycided emitter structure, and double-level metallization.

Addition of a bipolar transistor to a CMOS process provides the circuit designer with the capability to drive large capacitive loads with less cost in input capacitance and/or silicon area. Alternatively, because of the reduced sensitivity of gate delay to load capacitance, design can be simplified since the requirement for exact *a priori* estimates of circuit parasitics is eased. High-density BiCMOS SRAM's typically use a small number of bipolar transistors relative to the large number of CMOS devices comprising the memory array and periphery. Formation of the memory array and reduction of process complexity and defect density levels are of fundamental importance. The bipolar transistor must be added with minimal increase in process complexity while maintaining the technology as CMOS-like as possible.

An aggressive bit cell size of less than 20 μm^2 has been achieved with the introduction of an additional WSI_x polycide layer which forms self-aligned bit sense contact landing pads, a global interconnect to supply V_{ss} to the cell, and the emitter of the n-p-n bipolar transistors. The self-aligned contact landing pad relaxes the requirements for bit sense contact to word line and active edge spacing encountered in a conventional bit cell design.

II. Process Technology

The process that was developed is a CMOS-based 0.5-μm generation BiCMOS technology in which bipolar transistors were added to an existing 0.5-μm CMOS process. Growth of a thin epitaxial layer as well as addition of three masking steps; self-aligned buried layer, deep collector, and active base, were required to form the bipolar transistor. The original CMOS process featured self-aligned twin-well formation, framed mask poly-buffered LOCOS (FMPBL) isolation, a 150-Å gate, oxide thickness, surface-channel NMOS and buried-channel PMOS transistors, a reverse sequence, disposable polysilicon spacer module, three levels of polysilicon, and two layers of metallization. A large numerical aperture (NA = 0.54) G-line stepper was used for patterning all masking layers, resulting in pitches of 1.2 μm for gate polysilicon and 1.3 μm for active isolation.

The primary role of the bipolar transistor in this technology is to drive large capacitive loads in a BiCMOS gate configuration. To decrease the risk of bipolar saturation, a low collector resistance R_C is essential. Both an n^+ buried layer in a thin epitaxial region and a deep collector implant were added to the original CMOS process in order to minimize R_C. A self-aligned p^+ buried layer

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J. D. Hayden, T. C. Mele, A. H. Perera, D. Burnett, F. W. Walczyk, C. S. Lage, F. K. Baker, M. Woo, W. Paulson, M. Lien, and D. Denning are with Advanced Products Research and Development Laboratory, Motorola Inc., Austin, TX 78721.

Y. C. See and S. J. Cosentino are with Advanced Custom Technology Center, Motorola Inc., Mesa, AZ 85210.

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(or chan-stop) compensates the lateral diffusion and autodoping of the arsenic buried layer and reduces the n^+ to n^+ buried layer spacing at the expense of increased bipolar collector-substrate capacitance C_{CS} in the bipolar transistor. An offset between n^+ and p^+ buried layers will reduce C_{CS} but will increase process complexity, requiring an additional masking step and will increase the minimum required separation between n^+ buried layers.

A 1.6-μm thick lightly p-doped epitaxial layer was grown subsequent to buried-layer formation. The p doping as well as a heavier p-type cap layer are used to control arsenic autodoping. Thinner epitaxial layers, and well and field drives with reduced thermal cycles were developed to improve bipolar performance and reduce updiffusion of the buried layers. The final flat zone width is approximately 0.4 μm.

The self-aligned twin-well approach from the base CMOS process was retained; although, the temperature and time of subsequent thermal cycles was reduced to combat updiffusion of the buried layers.

To meet the needs of a high-density memory array for lower defect density levels and reduced process complexity, the isolation was maintained unchanged from the base CMOS process. This is at the cost of increased bipolar parasitic capacitances and reduced bipolar performance. A framed-mask poly-buffered LOCOS (FMPBL) isolation is used to achieve an active pitch of 1.3 μm and acceptable MOSFET narrow-width effects down to effective channel width of 0.25 μm [1], [2]. Gate oxide integrity and reliability were maintained relative to a standard LOCOS process, as indicated with time-zero breakdown and charge-to-breakdown measurements.

CMOS transistors are fabricated with a 150 Å gate oxide which provides a compromise between oxide reliability at 5-V operation and MOSFET short-channel behavior. Surface-channel NMOS and buried-channel PMOS transistors provide long-channel MOSFET characteristics down to effective channel lengths of 0.35 and 0.50 μm, respectively. Both transistor types use shallow threshold adjust and deeper punchthrough suppression implants. Moderately doped drain (MDD) regions are used for both NMOS and PMOS transistors to provide improved short-channel behavior. A reverse sequence, disposable polysilicon spacer module is used for MOSFET MDD formation to reduce the lateral encroachment of the source/drain regions and provide improved diode leakage [3].

Three levels of polysilicon are used in this process. The first layer is the gate electrode for the CMOS transistors. The second is a tungsten–polycide/polysilicon stack that performs three functions: creating self-aligned contact landing pads in the SRAM bit cell, forming the emitter of the n-p-n, and providing a global interconnect. The third polysilicon layer forms the teraohm resistor load for the bit cell.

The bipolar transistor is formed using the PMOS n well for the collector, the p^+ S/D implant as the extrinsic base contact, added implants for the active or intrinsic base region and the deep collector, and the second tungsten-polycide layer as the emitter. The extrinsic base and emitter regions are not self-aligned to each other. Allowing adequate margin for misalignment and dimensional variation, results in a large separation between extrinsic base and emitter. This translates into a relatively large base resistance R_B. The benefit of this approach is a simplified process in which lateral encroachment of the extrinsic base dopant is not a concern and design of a link base implant is not required. Reduced base-emitter breakdown voltage BV_{EBO} and enhanced bipolar hot carrier injection (HCI) effects are thus not an issue. The active base implant could be merged with the p-MDD implant without degrading PMOS characteristics. This implant, however, is also used to form the ECL load resistor and merging would reduce the freedom to adjust resistor values. The requirements of the PMOS transistor for a high n-well doping to suppress bulk punchthrough and the n-p-n bipolar for a low collector doping to ensure acceptable collector–base and collector–emitter breakdowns and reduced collector substrate capacitance were decoupled by the use of a PMOS punchthrough suppression implant. Placing this implant under the bipolar emitter–base junction also would serve to retard the onset of base pushout or the Kirk effect [4]. Alternatively, the selectively implanted collector or SIC [5] approach in which a deep n-type pocket is formed by an implant self-aligned to the emitter was investigated.

The polycide emitter and the self-aligned contact landing pad are formed simultaneously. Consequently, both are affected similarly by interfacial oxide and dopant loss during polycide formation. An HF dip is used prior to emitter polysilicon deposition to reduce the effect of any interfacial oxide. Additionally, the emitter is annealed with a rapid thermal anneal (RTA) which balls up interfacial oxide at the emitter polysilicon/silicon interface as well as activating the arsenic and driving it out of the emitter polysilicon.

Contacts are formed either using a conventional tapered etch process or with a straight-wall etch followed by a tungsten plug formation. The tungsten plugs are fabricated in the conventional fashion using a deposition plus etch-back process. The conventional TiN barrier is employed in either case. The patterned contact size is 0.6×0.6 μm^2.

Two levels of metallization are required in this process. The RTA emitter anneal also flows the BPSG layer below Metal 1. A photoresist deposition plus etchback technique is used for planarization between metal layers.

A schematic cross section of this technology is shown in Fig. 1 and a SEM cross-sectional micrograph in Fig. 2. In Fig. 1, NMOS, PMOS, and n-p-n bipolar transistors are schematically depicted and all three polysilicon layers are represented. The first polysilicon layer is used for the MOSFET gates. The second layer forms the self-aligned contact landing pad in the SRAM array as well as the bipolar emitter. The third polysilicon layer forms the load resistor for the bit cell. Fig. 2 is an actual cross section of the SRAM bit cell. All three polysilicon layers can

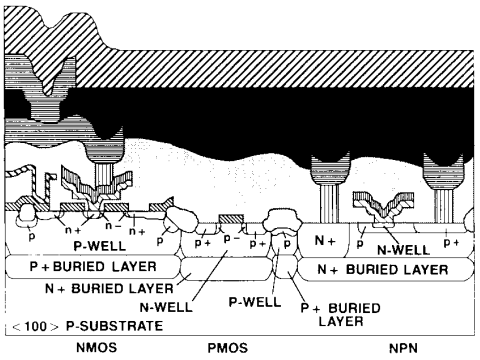

Fig. 1. Schematic cross section of the 0.5-μm BiCMOS technology.

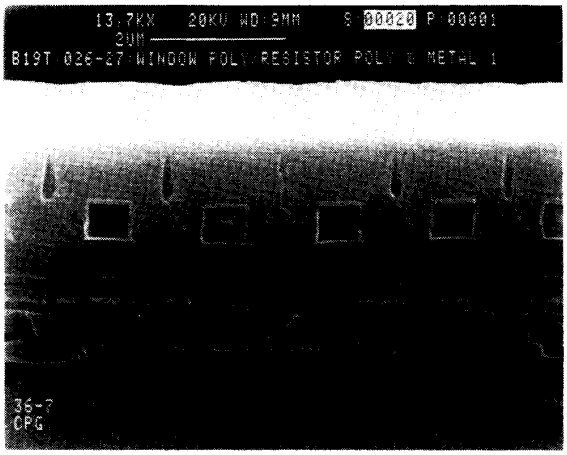

Fig. 2. SEM cross-sectional photomicrograph of the 0.5-μm BiCMOS technology.

again be seen. The second polysilicon layer acts here as both self-aligned contact and local interconnect. The first polysilicon layer forms the MOSFET gates and the third layer forms the bit cell load resistor.

III. CMOS Transistor Characteristics

Surface-channel NMOS and buried-channel PMOS devices are designed with nominal poly gate lengths of 0.70 and 0.90 μm and electrical or effective channel lengths L_{eff} of 0.50 and 0.65 μm, respectively. Long-channel behavior is maintained to minimum L_{eff} values of 0.35 and 0.50 μm. The NMOS and PMOS inverse subthreshold slopes ($|V_{DS}| = 5.0$ V) are 93 and 86 mV/decade, respectively, and off leakages ($|V_{DS}| = 5.0$ V) at minimum L_{eff} values are below 1 pA/μm as is illustrated in Fig. 3. Intrinsic gate delays of less than 100 ps/gate at a power supply voltage of 5.0 V have been obtained for unloaded CMOS ring oscillators. CMOS device characteristics are presented in Fig. 3 and summarized in Table I.

The triple-polysilicon technology allows a second polysilicon contact to the n^+ regions. The polysilicon contact adds little resistance, changing the drain saturation current by less than 2%, independent of whether the second polysilicon contact is placed at the source or drain terminal.

A reverse-sequence, disposable polysilicon spacer process has been used for MOSFET MDD formation [3] in order to reduce lateral encroachment of the MDD regions by approximately 0.05 μm per side.

IV. n-p-n Transistor Characteristics

The WSi_x polycide which forms the self-aligned contact landing pads in the bit cell is also used for the emitter of the n-p-n bipolar transistor. A schematic cross section of the bipolar transistor is shown in Fig. 4 and a SEM micrograph in Fig. 5. Fig. 6 is a high resolution TEM photomicrograph of the emitter polysilicon/silicon interface. The results of the emitter RTA anneal in which the interfacial oxide is "balled" up are apparent. Additionally, some degree of epitaxial realignment of the polysilicon film is typically observed.

A Gummel plot for the nominal n-p-n transistor with an emitter size of 0.8×2.4 μm^2 displays ideal base and collector I–V characteristics with a slope of 60 mV/decade down to current levels below 1 pA/μm^2 (Fig. 7). The bipolar transistor is designed for a current gain h_{FE} of 100, which is maintained over 7–8 orders of magnitude in collector current. The collector current at the onset of base push-out (knee current or I_K, defined at a 50% roll-off in h_{FE}) is approximately 500 μA/μm^2. The effects of bipolar saturation are reduced by maintaining a low collector resistance $R_{C\text{sat}}$ of 50 Ω. The peak cutoff frequency f_T is in excess of 12 GHz for the nominal transistor, where measurements are made at a constant collector-base voltage, V_{CB}, of 2.0 V and the peak in f_T occurs around 100–200 μA/μm^2. Emitter–base (BV_{EBO}), collector–base (BV_{CBO}), and collector–emitter breakdowns (BV_{CEO}) are maintained above 6.0, 18.0, and 6.5 V, respectively. Electrical parameters for the nominal WSi_x polycide emitter n-p-n device are listed in Table II.

Bipolar parasitic resistances and capacitances have in many instances been sacrificed for the sake of reduced process complexity. Non self-aligned emitter and extrinsic base regions result in larger base resistance R_B, and collector–base capacitance C_{CB}, but allow acceptable base–emitter breakdown voltage BV_{EBO}, and bipolar HCI resistance. Use of a LOCOS-type nonrecessed isolation degrades collector–substrate C_{CS} and collector–base C_{CB} capacitances. A self-aligned buried-layer process with a p^+ buried layer, while reducing n^+ to n^+ buried layer spacing, also degrades C_{CS}.

V. Epitaxial-Layer Thickness

The effect of epitaxial-layer thickness on bipolar transistor characteristics has been evaluated. A sensitivity analysis was performed in which the grown epitaxial layer thickness was varied from 1.4 to 1.95 μm while the implanted collector dose was maintained constant. The grown epitaxial layer thicknesses correlate to flat zone

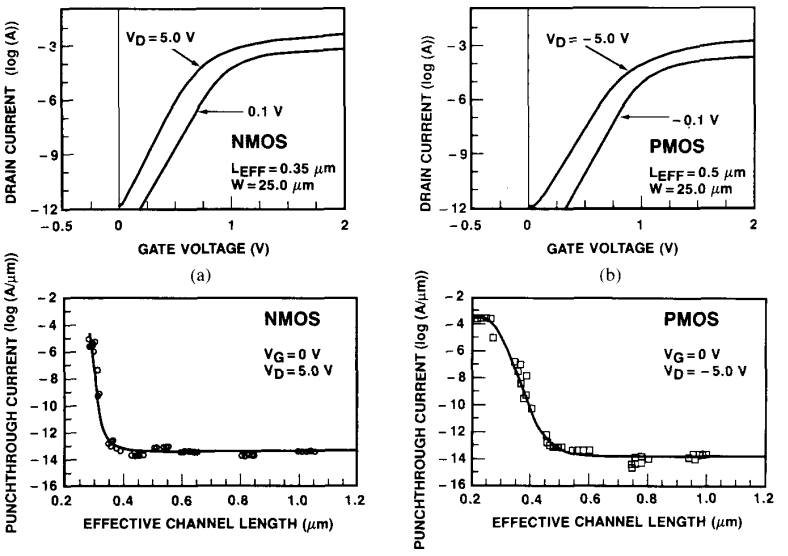

Fig. 3. CMOS transistor characteristics. (a), (c) are I_D versus V_{GS} curves at $|V_{DS}| = 0.1$ V, $|V_{DS}| = 5.0$ V for 0.35-μm NMOS and 0.50-μm PMOS transistors, respectively. (b), (d) are off-leakage currents (log $[I_D]$ at $V_G = 0$, $V_D = 5$ V) versus L_{eff}. The transistor widths are 25 μm in all figures.

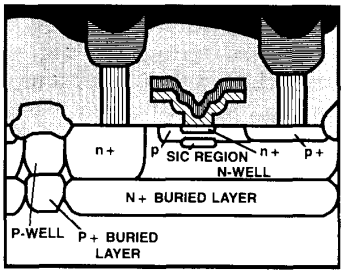

Fig. 4. Schematic cross section of the WSi_x polycide emitter n-p-n bipolar transistor. The location of the n-doping pocket created by the SIC implant is shown.

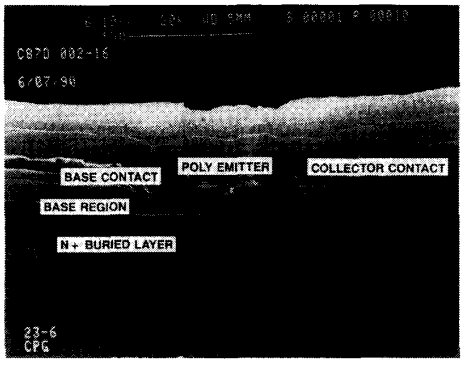

Fig. 5. SEM cross section of a WSi_x polycide emitter n-p-n transistor. The emitter area is 0.8×2.4 μm^2. The polycide is comprised of 2 kÅ WSi_x and 1 kÅ polysilicon.

TABLE I
CMOS TRANSISTOR PARAMETERS

Parameter	NMOS	PMOS
L_{EFF} [nominal] (μm)	0.50	0.65
V_T (V)	0.90	−1.0
I_{DS} [sat, nominal] (mA/μm)	0.43	0.19
SS^{-1} [nominal] (mV/dec.)	93	86

widths from 0.20 to 0.75 μm, respectively. Fig. 8 demonstrates the improvement in knee current (defined as the collector current for a 50% reduction in transistor gain h_{FE}) and gate delay of a loaded BiCMOS ring oscillator. The delay in the onset of base push-out or the Kirk effect is predicted theoretically [4] and has been reported in the literature [10]. The thinner epi reduces the component of the collector resistance under the intrinsic device and increases the collector current at the onset of quasi-saturation. Retardation of the onset of base push-out and quasi-saturation both serve to increase the ability of the bipolar

Fig. 6. TEM cross section of the emitter polysilicon/silicon interface showing balled up interfacial oxide as well as partial epitaxial regrowth.

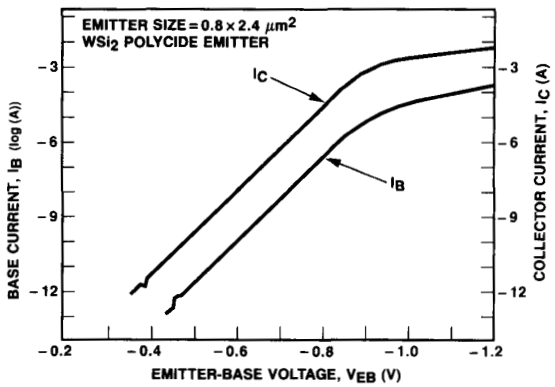

Fig. 7. Gummel plot for a nominal WSi_x polycide emitter n-p-n transistor. The emitter area is 0.8 × 2.4 μm^2. The polycide comprises 2 kÅ WSi_x and 1 kÅ polysilicon.

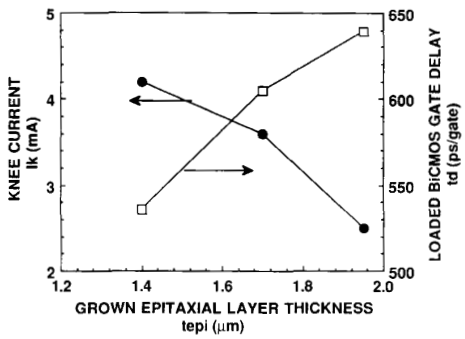

Fig. 8. Measured n-p-n bipolar knee current I_K and loaded BiCMOS gate delay as a function of epitaxial-layer thickness. The knee current is defined as the collector current for a 50% reduction in transistor gain.

TABLE II
n-p-n BIPOLAR TRANSISTOR CHARACTERISTICS
(The emitter area is 0.8 × 2.4 μm^2. The polycide comprises 2 kÅ WSi_x and 1 kÅ polysilicon.)

Parameter	Value
BV_{CBO}	18 V
BV_{CEO}	6.5 V
BV_{EBO}	6.0 V
C_{EB}	8 fF
C_{CB}	13 fF
C_{CS}	67 fF
R_E	25 Ω
f_T	14 GHz
h_{FE}	100

transistor to source large currents. This combination results in the observed reduction in BiCMOS gate delay. Fig. 9 indicates that there is a tradeoff between higher peak cutoff frequency and lower bipolar snapback voltage with thinner epitaxial layer thickness. The higher peak cutoff frequency f_T results from the delay in the onset of base push-out as well as a narrowing of the intrinsic base. The effective collector doping under the base is increased because a constant collector dose has been placed in a

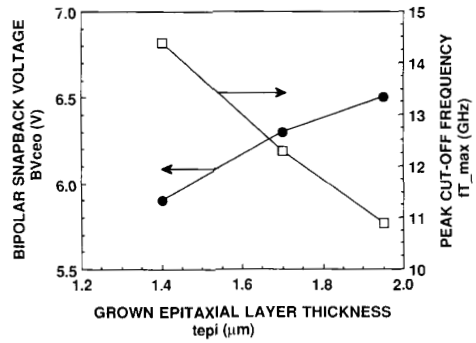

Fig. 9. Measured n-p-n bipolar snapback voltage BV_{CEO}, and peak cutoff frequency f_T, as a function of epitaxial layer thickness.

thinner epilayer and because of up-diffusion of the buried layer. The higher effective collector doping pinches the intrinsic base profile, increasing the peak cutoff frequency, f_T, the base Gummel number, and transistor gain h_{FE}. The higher effective collector doping and higher current gain both contribute to the observed reduction in the bipolar snapback voltage, BV_{CEO}.

VI. Optimization of the SIC Implant

The selectively ion implanted collector (SIC) [5] been proposed as a means of increasing cutoff frequency f_T and knee current I_K, without sacrificing collector–base capacitance C_{CB}. In the SIC approach, an n-type pocket, self-aligned to the emitter, is placed below the active base. This pocket cuts off the channeling tail from the boron implant, increasing f_T. Additionally, the higher n-type doping serves to delay the onset of base push-out or the Kirk effect [4]. The potential benefits of the SIC implant were investigated through extensive process and device simulation with PEPPER [6] and MEDUSA [7], respectively. Active base and SIC implant conditions were jointly optimized using a matrix of simulations based on an experimental design generated by the RS1 software package [8]. Fig. 10 shows simulated doping profiles through the intrinsic bipolar device with and without the SIC implant. Device simulations were performed to study current gain h_{FE}, peak cutoff frequency f_T, knee current (defined as the collector current for a 50% reduction in h_{FE}), I_K, and bipolar snapback voltage BV_{CEO}, as a function of active base and SIC implant dose and energy. Response surfaces were fit describing the dependence of these electrical parameters on the implant parameters and contour plots of the results of the device simulations were generated across the matrix of input parameters using RS1. These contour plots are shown in Figs. 11–14. Contour plots of cutoff frequency, knee current, and snapback voltage exhibit clear tradeoffs as implant conditions are varied. The primary dependence for f_T and I_K is on base implant energy. As the base implant energy is reduced, f_T increases while I_K decreases. A narrower base width decreases base transit time and improves peak cutoff frequency. A lower base implant energy results in more

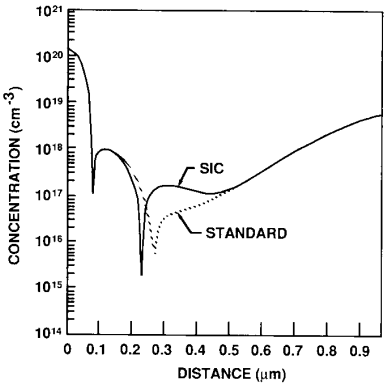

Fig. 10. Simulated doping profiles for the intrinsic bipolar transistor comparing the standard with the SIC devices.

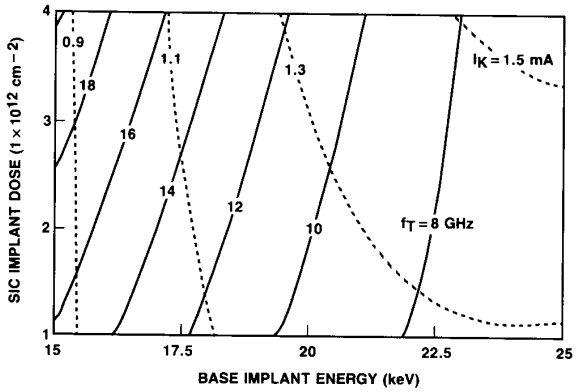

Fig. 11. Contour plots of simulated f_T and I_K characteristics for the nominal n-p-n device as functions of base implant energy and SIC dose. The base implant dose was 2 × 10^{13} cm^{-2} and SIC energy was 150 keV.

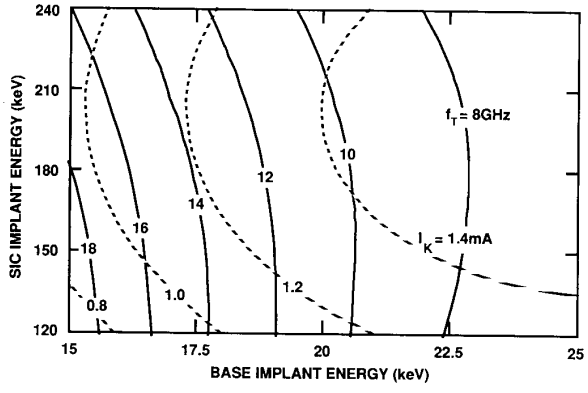

Fig. 12. Contour plots of simulated f_T and I_K characteristics for the nominal n-p-n device as functions of base implant energy and SIC implant energy. The base implant dose was 2 × 10^{13} cm^{-2} and SIC implant dose was 3 × 10^{12} cm^{-2}.

compensation of the base dopant by the emitter, lowering the peak base doping and lowering the threshold for the onset of high-level injection. Additionally, a shallower base profile implies a larger flat zone which lowers the

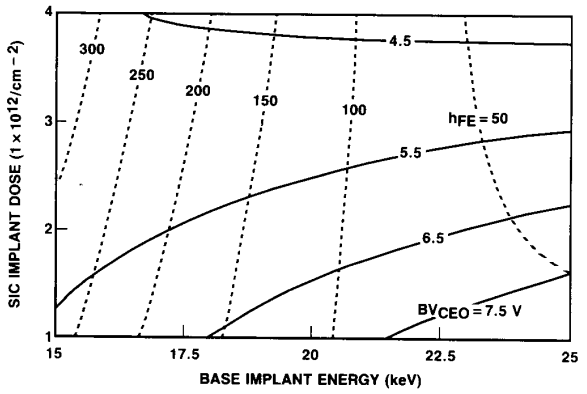

Fig. 13. Contour plots of simulated BV_{CEO} and h_{FE} characteristics for the nominal n-p-n device as functions of base implant energy and SIC implant dose, for a base dose of 2 × 10^{13} cm^{-2} and SIC energy of 150 keV.

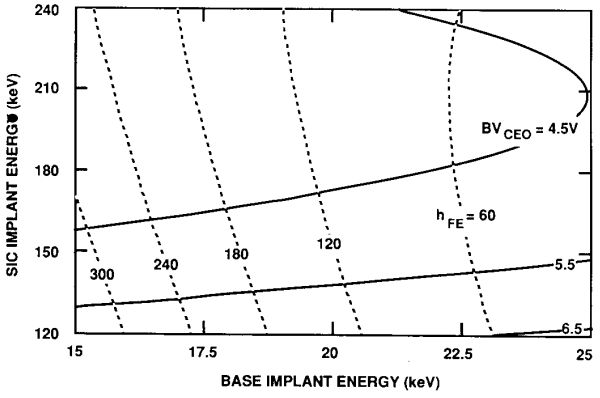

Fig. 14. Contour plots of simulated BV_{CEO} and h_{FE} characteristics for the nominal n-p-n device as functions of base implant energy and SIC implant energy. The base implant dose was 2 × 10^{13} cm^{-2} and SIC implant dose was 3 × 10^{12} cm^{-2}.

collector current required for the onset of base push-out or the Kirk effect. Higher SIC doses and lower SIC energies increase f_T by pinching off the base profile and reducing the base width. Higher SIC implant energies and doses improve the knee current by placing more n-type dopant below the intrinsic device and increasing the collector current required for the onset of the Kirk effect. By adjusting the SIC implant dose at fixed active base and SIC implant energies, I_K can be improved by approximately 20% as long as the base implant energy is above 20 keV. A lower SIC implant energy is required to improve I_K for lower energy base implants. Higher SIC implant doses degrade the bipolar snapback voltage because the heavier n-type doping lowers the collector–base breakdown voltage BV_{CBO} and, hence, BV_{CEO}. Lower SIC implant energies actually improve BV_{CEO} since more of the SIC implant is compensated by the base profile. Bipolar snapback tends to decrease with lower base implant energies. This correlates with the increase in transistor gain as the base Gummel number is reduced. Simulation

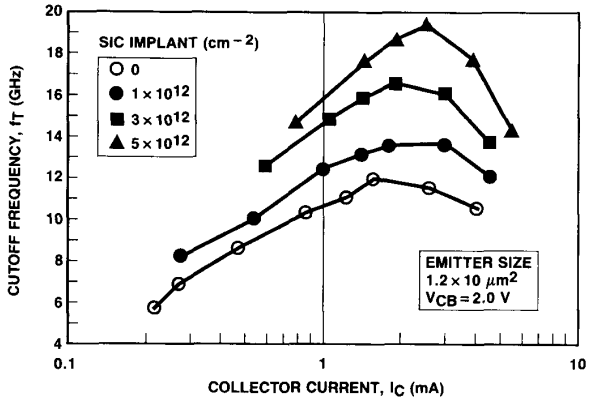

Fig. 15. Measured f_T versus I_C characteristics illustrating the effect of the SIC implant on peak cutoff frequency. The emitter area is 1.2 × 10 μm^2 and V_{CB} = 2.0 V.

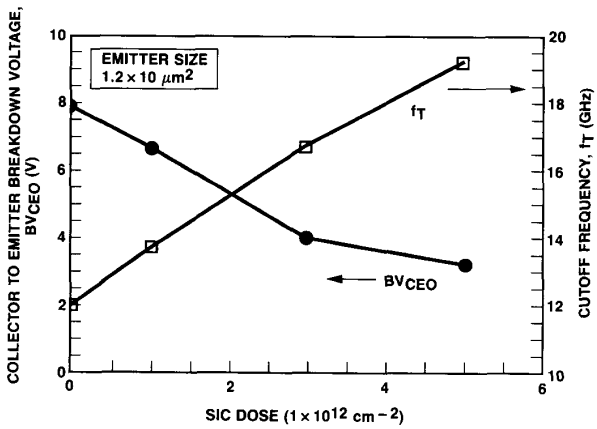

Fig. 16. Measurements of f_T and BV_{CEO} as function of the SIC implant dose. The emitter area is 1.2 × 10 μm^2.

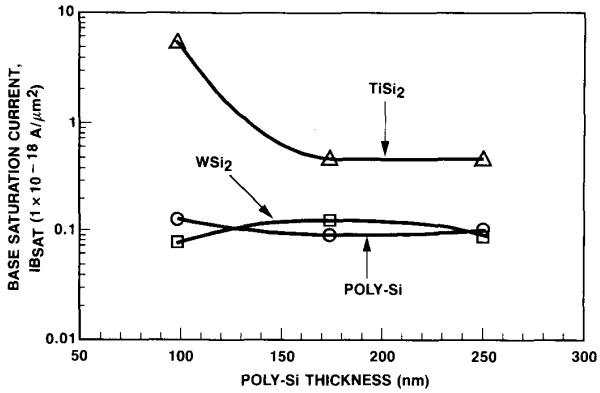

Fig. 17. n-p-n base saturation current I_{BSAT} versus the emitter polysilicon thickness for the three emitter structures. The WSi_x thickness was 2 kÅ and the $TiSi_2$ thickness was 500 Å.

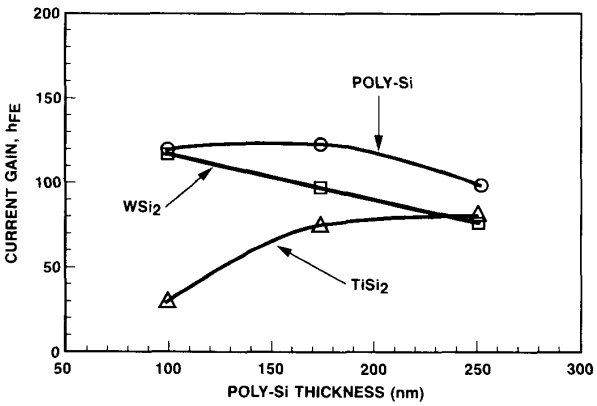

Fig. 18. n-p-n peak current gain h_{FE} versus emitter polysilicon thickness for the three emitter structures. The WSi_x thickness was 2 kÅ and the $TiSi_2$ thickness was 500 Å.

results indicate that an improvement in I_K is expected to be coupled with the reduced BV_{CEO}.

The selectively ion implanted collector (SIC) was also investigated experimentally. Fig. 15 is a plot of peak cutoff frequency versus collector current for a series of SIC implant doses. The SIC implant increases f_T from 12 GHz with no implant to a maximum of 19 GHz. Fig. 16 demonstrates that the improved cutoff frequency must be traded off against a lower bipolar snapback voltage BV_{CEO}. A peak cutoff frequency of 14 GHz can be achieved while maintaining a BV_{CEO} of 6.5 V.

VII. Tungsten Polycide

The emitter polysilicon layer must be strapped with a silicide to provide a low sheet resistance interconnect for the V_{SS} connection in the bit cell. A WSi_x polycide and a $TiSi_2$ salicide were compared experimentally. The impact of adding a $TiSi_2$ or WSi_x layer on top of the emitter polysilicon was evaluated by examining the n-p-n transistor characteristics as a function of emitter polysilicon thickness and emitter rapid thermal anneal (RTA) sequence. Formation of a $TiSi_2$ salicide on the emitter polysilicon caused a significant increase in base saturation current (IB_{SAT}) and decrease in transistor gain h_{FE} as the emitter polysilicon thickness was decreased. WSi_x polycide only slightly affected the n-p-n characteristics. This is illustrated in Figs. 17 and 18. When the $TiSi_2$ formation is performed prior to the emitter RTA anneal, the structure of the polysilicon emitter is dramatically affected. During salicidation, a large portion of the arsenic implanted into the emitter is lost due to arsenic segregation and consumption during the $TiSi_2$ reaction. This results in a reduction in the arsenic dopant segregated at the polysilicon/silicon interface which in turn reduces the effectiveness of the blocking layer or potential barrier at the polysilicon/silicon interface [9]. The lower potential barrier causes devices with $TiSi_2$ strapped emitters to become more susceptible to the effects of reducing the final emitter polysilicon thickness. As the polysilicon thickness approaches the hole minority-carrier diffusion length in the polysilicon emitter, an increase in IB_{SAT} is observed [9]. The thermal stability of the $TiSi_2$ layer is also an is-

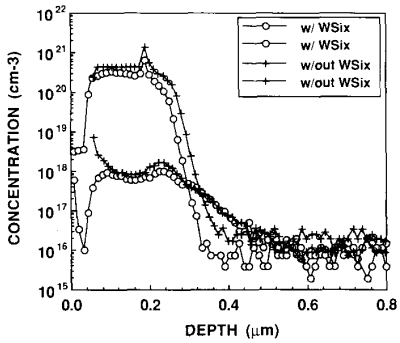

Fig. 19. SIMS profiles for emitter and base regions of n-p-n bipolar with polysilicon and WSi_x polycide emitters.

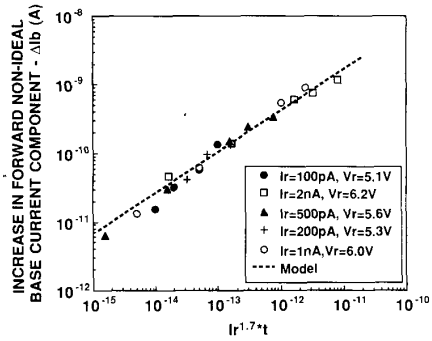

Fig. 20. Increase in nonideal base current component ΔI_B as a function of $I_R^{1.7} * t$ under band-to-band tunneling conditions.

sue. Performing the RTA emitter anneal after formation of the $TiSi_2$, will often result in agglomeration of $TiSi_2$. In WSi_x polycide devices, some arsenic segregation also occurs, but to a lesser extent. Fig. 19 compares the SIMS profiles for the polysilicon and the WSi_x polycide emitter n-p-n transistors. Because of arsenic segregation, the WSi_x device has a shallower emitter and thus a wider base and larger base Gummel number. The result is a decrease in transistor gain h_{FE} and emitter resistance R_E. The tungsten polycide also exhibited superior thermal stability, exhibiting negligible degradation after the RTA emitter anneal.

VIII. Bipolar HCI

It is well known that under reverse-bias emitter–base stress, bipolar transistors undergo HCI (hot carrier injection) degradation which is manifested as an increase in the nonideal base current component and a decrease in the low current gain [11]. Physically, charge is injected into the oxide above the emitter–base junction edge. This results in an increase in the density of interface states (DIT) above the junction edge, which contribute a recombination leakage component to the overall current. In standard operation of a BiCMOS gate, the emitter–base junctions of the bipolar transistors are transiently reverse-biased and bipolar HCI is hence a significant concern. A comprehensive study was carried out of HCI degradation in the bipolar transistors fabricated in this process. Earlier work was confirmed in which the generation of HCI damage is a function of the level of reverse bias stress the device is subjected to. In particular, when bipolar transistors experience a low-level stress corresponding to the band-to-band tunneling region of the reverse emitter–base breakdown characteristic, the nonideal base current component increases as $I_r^{1.7} * t$, as shown in Fig. 20. When the bipolar transistors are stressed under avalanche breakdown conditions, the nonideal base current component ΔI_B increases as a function of the total stress charge Q. Here, Q is equal to the product of the stress current and total stress time. This is illustrated in Fig. 21. In Fig. 22, the results of bipolar HCI stress under band-to-band tunneling and avalanche breakdown conditions are combined and the time for 50% beta degradation is plotted as a function of reverse stress current for different emitter–base forward

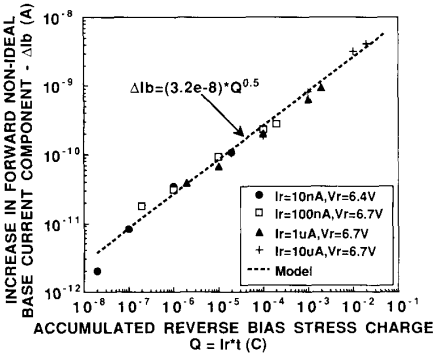

Fig. 21. Increase in nonideal base current component ΔI_B as a function of the total reverse stress charge $Q = I_R * t$ under reverse emitter–base junction avalanche breakdown conditions.

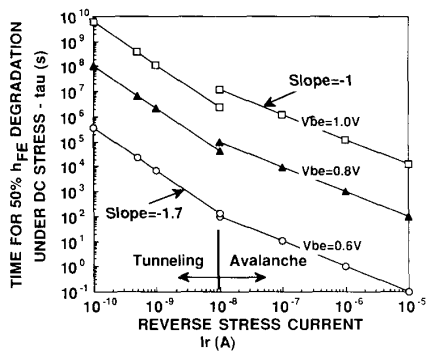

Fig. 22. The time to 50% reduction in transistor gain h_{FE} as a function of reverse bias stress current.

biases. It should be noted that the bipolar HCI stressing was carried out under dc conditions whereas the typical emitter–base reverse bias stress a bipolar transistor is subjected to is a transient waveform and the resulting duty cycle is quite low.

IX. ECL Ring Oscillator Measurements

ECL gate delay was measured as a means of characterizing bipolar performance. Fig. 23 compares gate delay to ECL ring oscillators with single- and double-base n-p-n bipolar transistors laid out with conservative design

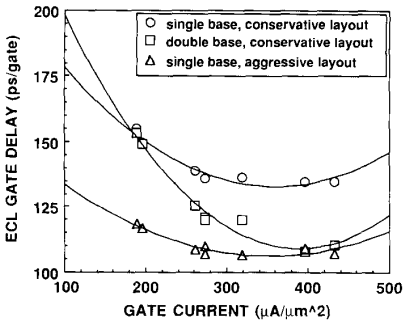

Fig. 23. Measured ECL gate delay as a function of gate current. The plot compares oscillators with single- and double-base bipolar transistors laid out with conservative design rules and single-base bipolar transistors laid out with aggressive design rules.

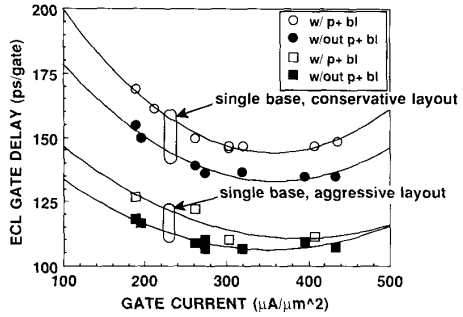

Fig. 24. Measured ECL gate delay as a function of gate current. The plot demonstrates the effect the p^+ buried layer has in increasing collector–substrate capacitance C_{CS} and degrading ECL gate delay.

rules and single-base n-p-n bipolar transistors laid out with aggressive design rules. The single-base n-p-n with aggressive design rules achieves an ECL gatedelay of 105 ps/gate at a gate current of 350 $\mu A/\mu m^2$. An ECL ring oscillator with double-base n-p-n bipolar transistors laid out with aggressive design rules would exhibit even faster gate delays. Increased process complexity in the form of a more recessed isolation, a lithographic offset between n^+ and p^+ buried layers, and a double-polysilicon, fully self-aligned bipolar structure, would provide improved ring oscillator performance, at the expense of reduced SRAM yield.

The impact of the p^+ buried layer in increasing the peripheral component of the collector–substrate capacitance C_{CS} was investigated. Fig. 24 demonstrates that leaving out the p^+ buried-layer implant improves ECL gate delay by approximately 10%. This is at the expense of increasing the minimum n^+ buried layer to n^+ buried spacing from 2.5 to 6.5 μm.

X. Conclusions

A high-performance 0.5-μm BiCMOS technology has been demonstrated which uses a triple-polysilicon process architecture for a fast 4-Mb SRAM class of products. Three layers of polysilicon were used to achieve a compact four transistor bit cell size that is less than 20 μm^2 by forming self-aligned bit-sense and V_{ss} contacts. A WSi_x polycide emitter n-p-n transistor was implemented with an emitter area of 0.8 × 2.4 μm^2 and peak cutoff frequency of 14 GHz. A selectively ion-implanted collector was used to compensate the base channeling tail as well as increase cutoff frequency and knee current while maintaining a collector-to-emitter breakdown voltage of 6.5 V. n-p-n base and SIC implant conditions were optimized through device simulations coupled with statistical experimental design. A minimum ECL gate delay of 105 ps was achieved at a gate current of 350 $\mu A/\mu m^2$.

Acknowledgment

Special thanks are extended to the APRDL CMOS SRAM group for their collaboration on the 0.5-μm CMOS array technology, to L. Parker and C. Gunderson for their assistance with last minute measurements, and to J. Teplik and V. de la Torre of ATC for technical discussions. The authors would also like to acknowledge R. Sivan and L. Parrillo for their guidance throughout this project. And finally, the authors would like to thank the APRDL manufacturing, process, and test engineering groups.

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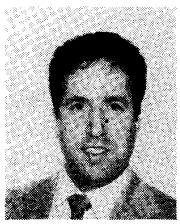
James D. Hayden (S'81-M'83-SM'91) received the B.S. degree in engineering physics from the University of Colorado, Boulder, and the M.S.E.E. degree from the University of Arizona, Tucson.

He worked as an RF Test Engineer at Bell Aerospace from 1981 to 1983. In 1983 he joined Advanced Micro Devices as a Modeling Engineer, developing circuit simulation models for EPROM and EEPROM products. From 1985 to 1986 he worked at NCR Microelectronics in Col-

orado Springs, CO, with device design responsibilities in the development of a 1-μm CMOS process. In 1987 he joined INMOS Corporation as a Device Physicist, working on the development of 1.2- and 0.8-μm SRAM processes. Since May 1988 he has worked at Motorola's Advanced Products Research and Development Laboratories, Austin, TX. His duties have included bipolar and MOS device design and SRAM bit cell development for 0.50- and 0.35-μm BiCMOS processes. He has authored or coauthored over 25 papers and holds 5 US patents.



Thomas C. Mele (S'83–M'88) was born in Ann Arbor, MI, on March 31, 1961. He received the B.S. degree (Magna Cum Laude) in electrical engineering from the University of Delaware, Newark, in 1983. While attending the University of Delaware he received The Outstanding Student of the Year Award from the College of Engineering in 1982 and the IEEE Engineering Award in 1983. He performed his doctoral studies at Cornell University, Ithaca, NY, and received the Ph.D. degree in electrical engineering in 1988.

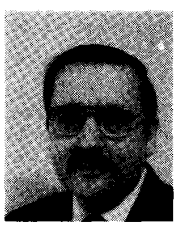
In 1988, he joined Motorola Inc., Austin, TX, as a member of the Advanced Products Research and Development Laboratory. He has since been involved in process integration for 0.5-μm CMOS and BiCMOS fast SRAM's. His specific projects have included salicide and local interconnect, test vehicle designs for process and device development, and baseline process integration for the 0.5-μm BiCMOS SRAM's. He is presently Section Manager of the APRDL Diffusion/Epi Process Engineering Group. His current research interests include the application of statistical experimental design techniques to develop and optimize VLSI processes, devices, and circuits.

Dr. Mele is a member of Tau Beta Pi, Eta Kappa Nu, and Phi Kappa Phi.

Asanga H. Perera, photograph and biography not available at the time of publication.

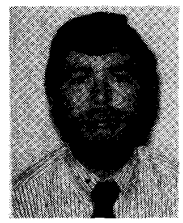
David Burnett received the B.S.E.E. from Texas A&M University, College Station, in 1984, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 1986 and 1990. His thesis focused on the reliability of bipolar devices.

In 1990, he joined the Advanced Products Research and Development Laboratory of Motorola in Austin, TX, working on a 0.5-μm BiCMOS technology for SRAM's.



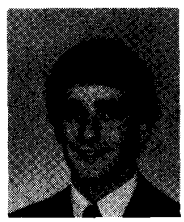
Fred W. Walczyk was born in Fall River, MA, in 1947. He received the B.S. degree from the University of Massachusetts at Dartmouth in 1969 and the M.S. degree from Bowling Green State University, Bowling Green, OH, in 1979, both in physics.

In 1969 he joined Texas Instruments to do development for radiation tolerant bipolar and J-FET devices. In 1980 he joined Digital Equipment Corporation where he engaged in CMOS and BiCMOS process development and integration for custom microprocessors. Since 1984 he has been with Motorola working on advanced CMOS and BiCMOS process integration and device engineering projects including nonvolatile and SRAM memory development.

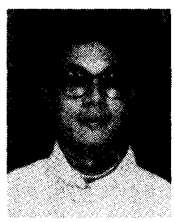


Craig S. Lage received the B.S. degree in physics from the California Institute of Technology, Pasadena, in 1976, and the M.S. degrees in nuclear engineering and electrical engineering from the University of Wisconsin at Madison in 1978 and 1979.

He was employed at Hewlett-Packard in Corvallis, OR, from 1979 until 1985, doing process integration work on CMOS technologies. In 1985 he joined Fairchild Semiconductor in Puyallup, WA (subsequently acquired by National Semiconductor), where he and his coworkers developed technology used for high-speed BiCMOS 256K and 1 Mb SRAM's. Since 1990 he has been with Motorola's Advanced Products Research and Development Laboratory in Austin, TX, working on high-speed BiCMOS SRAM technology.



Frank K. Baker was born in Fort Stockton, TX, on January 25, 1961. He received the B.Sc. degree in 1984 from the University of Texas, Austin, and the Master's degree in 1985 from Stanford University, both in electrical engineering. Since 1985, he has been a member of the Motorola, Inc. Advanced Products Research and Development Laboratory (APRDL) in Austin, TX. He has contributed in the areas of MOSFET design and process integration for 1.2-, 0.8-, and 0.5-μm SRAM technologies. His research interests include submicrometer device design, process integration and the reduction of hot carrier effects. He is currently serving as section manager for the 4M CMOS SRAM program in APRDL.



Michael Woo received the B.S. degree in chemical engineering from the University of Michigan, Ann Arbor, in 1984.

Since 1987, he has been a process development engineer at Motorola's Advanced Products Research and Development Laboratory in Austin, TX. He has published more than 10 papers and obtained 5 patents on the subjects of process integration and fine-line etching.

Wayne Paulson, photograph and biography not available at the time of publication.

Mitch Lien, photograph and biography not available at the time of publication.

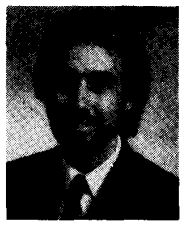
Yee-Chaung See (S'75–M'80–SM'90) received the B.S. degree in physics from National Taiwan University in 1971, the M.S. degrees in physics and in electrical engineering from Carnegie-Mellon University, Pittsburgh, PA in 1975 and the Ph.D. degree in electrical engineering from University of Pittsburgh, Pittsburgh, PA, in 1980.

From 1980 to 1983, he was a member of the technical staff at the Semiconductor Process and Design Center, Texas Instruments, Inc. His development efforts involved advanced CMOS technology, plasma etch, and $TiSi_2$ salicide. In 1983, he joined Motorola Inc. in Austin, TX. He was a device engineering manager in MOS8, responsible for the start up of the 2- and 1.5-μm products, the transfer of the 1.2-μm EPROM and SRAM processes and the establishment of the CMOS product transfer methodology. In 1987 he joined the Advanced Products Research and Development Laboratory as a manager of advanced development involved with the joint development with Toshiba Corp. From 1988 to 1989, he was responsible for the successful technology development and fabri-

cation of the 0.5-μm "Superchip" for the VHSIC Phase-II program. Since mid-1989, he has been managing the 0.5-μm BiCMOS technology development for the high-speed SRAM applications. In October 1990, he moved to the Advanced Technology Center in Mesa, AZ, where he is a manager of advanced development responsible for sub-0.5-μm BiCMOS and SiGe technology. Currently he is a senior member of the technical staff.

Dean Denning was born in Denver, CO, on October 19, 1961. He received the B.S. degree in chemical engineering in 1983 from the University of New Mexico in Albuquerque.

He joined Motorola Inc. Austin, TX, in 1988 as a member of the Advanced Products Research and Development Laboratory. His specific projects have primarily focused on LPCVD and RPCVD process development for current and future generation devices.



Stephen J. Cosentino (M'83) was born in England on February 26, 1955. He received the B.S. degree in physics in 1977 and the M.S. degree in electrical engineering in 1980, both from the University of Arizona at Tucson.

He joined Motorola's Advanced Products Research and Development Laboratory in 1979 where he was involved in the development of advanced NMOS and CMOS technologies for fast Static RAM products. In 1986, he joined the Advanced Custom Technology Center in Mesa, AZ, where he has been involved in the development of advanced BiCMOS technologies for fast Static RAM's and ASIC's. His current research activities include the development of advanced sub-0.5-μm BiCMOS technologies for high-performance ASIC's and telecommunications products. He is a Member of the Technical Staff, holds or co-holds 7 patents and has co-authored 12 technical publications.

Mr. Cosentino is a member of Phi Beta Kappa and the IEEE Electron Devices Society.