A High-Performance 0.5-μm BiCMOS Technology for Fast 4-Mb SRAM's

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Abstract—A high-performance 0.5-μm BiCMOS technology has been developed for a fast 4-Mb SRAM class of circuits. Three layers of polysilicon are used to achieve a compact four transistor SRAM bit cell of less than 20 μm² by creating self-aligned bit-sense and Vc contacts. A WSI, polycide emitter n-p-n transistor with an emitter area of 0.8 x 2.4 μm² provides a peak cutoff frequency (fT) of 14 GHz with a collector-emitter breakdown voltage (BVCEO) of 6.5 V. A selectively ion-implanted collector (SIC) is used to compensate the base channel tail in order to increase fT and knee current without significantly affecting collector-substrate capacitance. ECL gate delays as fast as 105 ps are obtained with this process.

I. INTRODUCTION

A 0.5-μm BiCMOS technology designed to support a high-performance fast 4-Mb SRAM class of products must satisfy a number of requirements. The SRAM bitcell area must be less than 20 μm² to meet package size constraints. The active transistors, and particularly the gate oxide thickness, must be designed to support a 5-V power supply. The NMOS and PMOS transistors should exhibit acceptable MOSFET behavior for minimum effective channel lengths of 0.35 and 0.5 μm, respectively. To maintain the performance advantage of bipolar over CMOS, the n-p-n transistor should have a peak cut off frequency fT exceeding 10 GHz while the bipolar snapback voltage BVCEO is maintained above 6.5 V. To satisfy all of these requirements, a 0.5-μm BiCMOS technology has been developed that combines a triple polysilicon process architecture with Framed Mask Poly-Buffered LOCOS (FMPBL) isolation [1], a disposable poly spacer module, a polycide emitter structure, and double-level metallization.

Addition of a bipolar transistor to a CMOS process provides the circuit designer with the capability to drive large capacitive loads with less cost in input capacitance and/or silicon area. Alternatively, because of the reduced sensitivity of gate delay to load capacitance, design can be simplified since the requirement for exact a priori estimates of circuit parasitics is eased. High-density BiCMOS SRAM's typically use a small number of bipolar transistors relative to the large number of CMOS devices comprising the memory array and periphery. Formation of the memory array and reduction of process complexity and defect density levels are of fundamental importance. The bipolar transistor must be added with minimal increase in process complexity while maintaining the technology as CMOS-like as possible.

An aggressive bit cell size of less than 20 μm² has been achieved with the introduction of an additional WSI, polycide layer which forms self-aligned bit sense contact landing pads, a global interconnect to supply Vss to the cell, and the emitter of the n-p-n bipolar transistors. The self-aligned contact landing pad relaxes the requirements for bit sense contact to word line and active edge spacing encountered in a conventional bit cell design.

II. PROCESS TECHNOLOGY

The process that was developed is a CMOS-based 0.5-μm generation BiCMOS technology in which bipolar transistors were added to an existing 0.5-μm CMOS process. Growth of a thin epitaxial layer as well as addition of three masking steps; self-aligned buried layer, deep collector, and active base, were required to form the bipolar transistor. The original CMOS process featured self-aligned twin-well formation, framed mask poly-buffered LOCOS (FMPBL) isolation, a 150-Å gate, oxide thickness, surface-channel NMOS and buried-channel PMOS transistors, a reverse sequence, disposable polysilicon spacer module, three levels of polysilicon, and two layers of metallization. A large numerical aperture (NA = 0.54) G-line stepper was used for patterning all masking layers, resulting in pitches of 1.2 μm for gate polysilicon and 1.3 μm for active isolation.

The primary role of the bipolar transistor in this technology is to drive large capacitive loads in a BiCMOS gate configuration. To decrease the risk of bipolar saturation, a low collector resistance Rc is essential. Both an n⁺ buried layer in a thin epitaxial region and a deep collector implant were added to the original CMOS process in order to minimize Rc. A self-aligned p⁺ buried layer
(or chan-stop) compensates the lateral diffusion and autodoping of the arsenic buried layer and reduces the $n^+$ to $n^-$ buried layer spacing at the expense of increased bipolar collector-substrate capacitance $C_{cs}$ in the bipolar transistor. An offset between $n^+$ and $p^+$ buried layers will reduce $C_{cs}$ but will increase process complexity, requiring an additional masking step and will increase the minimum required separation between $n^+$ buried layers.

A 1.6-$\mu$m thick lightly $p$-doped epitaxial layer was grown subsequent to buried-layer formation. The $p$ doping as well as a heavier $p$-type cap layer are used to control arsenic autodoping. Thinner epitaxial layers, and well and field drives with reduced thermal cycles were developed to improve bipolar performance and reduce updiffusion of the buried layers. The final flat zone width is approximately 0.4 $\mu$m.

The self-aligned twin-well approach from the base CMOS process was retained; although, the temperature and time of subsequent thermal cycles was reduced to combat updiffusion of the buried layers.

To meet the needs of a high-density memory array for lower defect density levels and reduced process complexity, the isolation was maintained unchanged from the base CMOS process. This is at the cost of increased bipolar parasitic capacitances and reduced bipolar performance.

A framed-mask poly-buffered LOCOS (FMPBL) isolation is used to achieve an active pitch of 1.3 $\mu$m and acceptable MOSFET narrow-width effects down to effective channel width of 0.25 $\mu$m [1], [2]. Gate oxide integrity and reliability were maintained relative to a standard LOCOS process, as indicated with time-zero breakdown and charge-to-breakdown measurements.

CMOS transistors are fabricated with a 150 $\AA$ gate oxide which provides a compromise between oxide reliability at 5-V operation and MOSFET short-channel behavior. Surface-channel NMOS and buried-channel PMOS transistors provide long-channel MOSFET characteristics down to effective channel lengths of 0.35 and 0.50 $\mu$m, respectively. Both transistor types use shallow threshold adjust and deeper punchthrough suppression implants. Moderately doped drain (MDD) regions are used for both NMOS and PMOS transistors to provide improved short-channel behavior. A reverse sequence, disposable polysilicon spacer module is used for MOSFET MDD formation to reduce the lateral encroachment of the source/drain regions and provide improved diode leakage [3].

Three levels of polysilicon are used in this process. The first layer is the gate electrode for the CMOS transistors. The second is a tungsten-poly-silicon/polysilicon stack that performs three functions: creating self-aligned contact landing pads in the SRAM bit cell, forming the emitter of the n-p-n, and providing a global interconnect. The third polysilicon layer forms the terahm resistor load for the bit cell.

The bipolar transistor is formed using the PMOS n well for the collector, the $p^+$ S/D implant as the extrinsic base contact, added implants for the active or intrinsic base region and the deep collector, and the second tungsten-poly-silicon layer as the emitter. The extrinsic base and emitter regions are not self-aligned to each other. Allowing adequate margin for misalignment and dimensional variation, results in a large separation between extrinsic base and emitter. This translates into a relatively large base resistance $R_b$. The benefit of this approach is a simplified process in which lateral encroachment of the extrinsic base dopant is not a concern and design of a link base implant is not required. Reduced base-emitter breakdown voltage $BV_{BEO}$ and enhanced bipolar hot carrier injection (HCI) effects are thus not an issue. The active base implant could be merged with the p-MDD implant without degrading PMOS characteristics. This implant, however, is also used to form the ECL load resistor and merging would reduce the freedom to adjust resistor values. The requirements of the PMOS transistor for a high n-well doping to suppress bulk punchthrough and the n-p-n bipolar for a low collector doping to ensure acceptable collector-base and collector-emitter breakdowns and reduced collector substrate capacitance were decoupled by the use of a PMOS punchthrough suppression implant. Placing this implant under the bipolar emitter-base junction also would serve to retard the onset of base pushout or the Kirk effect [4]. Alternatively, the selectively implanted collector or SIC [5] approach in which a deep n-type pocket is formed by an implant self-aligned to the emitter was investigated.

The poly-silicon emitter and the self-aligned contact landing pad are formed simultaneously. Consequently, both are affected similarly by interfacial oxide and dopant loss during poly-silicon formation. An HF dip is used prior to emitter polysilicon deposition to reduce the effect of any interfacial oxide. Additionally, the emitter is annealed with a rapid thermal anneal (RTA) which ball up interfacial oxide at the emitter polysilicon/silicon interface as well as activating the arsenic and driving it out of the emitter polysilicon.

Contacts are formed either using a conventional tapered etch process or with a straight-wall etch followed by a tungsten plug formation. The tungsten plugs are fabricated in the conventional fashion using a deposition plus etch-back process. The conventional TiN barrier is employed in both cases. The patterned contact size is 0.6 $\times$ 0.6 $\mu$m$^2$.

Two levels of metallization are required in this process. The RTA emitter anneal also flows the BPSG layer below Metal 1. A photore sist deposition plus etchback technique is used for planarization between metal layers.

A schematic cross section of this technology is shown in Fig. 1 and a SEM cross-sectional micrograph in Fig. 2. In Fig. 1, NMOS, PMOS, and n-p-n bipolar transistors are schematically depicted and all three polysilicon layers are represented. The first polysilicon layer is used for the MOSFET gates. The second layer forms the self-aligned contact landing pad in the SRAM array as well as the bipolar emitter. The third polysilicon layer forms the load resistor for the bit cell. Fig. 2 is an actual cross section of the SRAM bit cell. All three polysilicon layers can
rent by less than 2%, independent of whether the second polysilicon contact is placed at the source or drain terminal.

A reverse-sequence, disposable polysilicon spacer process has been used for MOSFET MDD formation [3] in order to reduce lateral encroachment of the MDD regions by approximately 0.05 pm per side.

IV. n-p-n TRANSISTOR CHARACTERISTICS

The WSi, polycide which forms the self-aligned contact landing pads in the bit cell is also used for the emitter of the n-p-n bipolar transistor. A schematic cross section of the bipolar transistor is shown in Fig. 4 and a SEM micrograph in Fig. 5. Fig. 6 is a high resolution TEM photomicrograph of the emitter polysilicon/silicon interface. The results of the emitter RTA anneal in which the interfacial oxide is “ballled” up are apparent. Additionally, some degree of epitaxial realignment of the polysilicon film is typically observed.

A Gummel plot for the nominal n-p-n transistor with an emitter size of 0.8 × 2.4 μm² displays ideal base and collector I-V characteristics with a slope of 60 mV/decade down to current levels below 1 pA/μm² (Fig. 7). The bipolar transistor is designed for a current gain hFE of 100, which is maintained over 7-8 orders of magnitude in collector current. The collector current at the onset of base push-out (knee current or IB, defined at a 50% roll-off in hFE) is approximately 500 μA/μm². The effects of bipolar saturation are reduced by maintaining a low collector resistance Re, of 50 Ω. The peak cutoff frequency f1 is in excess of 12 GHz for the nominal transistor, where measurements are made at a constant collector-base voltage, VCB, of 2.0 V and the peak in f1 occurs around 100–200 μA/μm². Emitter-base (BVCEO), collector-base (BVCEO), and collector-emitter breakdowns (BVCEO) are maintained above 6.0, 18.0, and 6.5 V, respectively. Electrical parameters for the nominal WSi, polycide emitter n-p-n device are listed in Table I.

Bipolar parasitic resistances and capacitances have in many instances been sacrificed for the sake of reduced process complexity. Non self-aligned emitter and extrinsic base regions result in larger base resistance Rb, and collector-base capacitance Cbb, but allow acceptable base-emitter breakdown voltage BVCEO, and bipolar HCL resistance. Use of a LOCOS-type nonrecessed isolation degrades collector-substrate Ccs and collector-base Ccb capacitances. A self-aligned buried-layer process with a p⁺ buried layer, while reducing n⁻ to n⁺ buried layer spacing, also degrades Ccs.

V. EPITAXIAL-LAYER THICKNESS

The effect of epitaxial-layer thickness on bipolar transistor characteristics has been evaluated. A sensitivity analysis was performed in which the grown epitaxial layer thickness was varied from 1.4 to 1.95 μm while the implanted collector dose was maintained constant. The grown epitaxial layer thicknesses correlate to flat zone...
Fig. 3. CMOS transistor characteristics. (a), (c) are $I_D$ versus $V_{GS}$ curves at $V_{DS} = 0.1$ V, $V_{DS} = 5.0$ V for 0.35-µm NMOS and 0.50-µm PMOS transistors, respectively. (b), (d) are off-leakage currents ($\log [I_O]$) at $V_C = 0$, $V_D = 5$ V) versus $L_{eff}$. The transistor widths are 25 µm in all figures.

Fig. 4. Schematic cross section of the WSi$_3$ polycide emitter n-p-n bipolar transistor. The location of the n-doping pocket created by the SIC implant is shown.

![Schematic cross section of WSi$_3$ polycide emitter n-p-n bipolar transistor](image)

**TABLE I**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
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<td>$L_{eff}$ [nominal] (µm)</td>
<td>0.50</td>
<td>0.65</td>
</tr>
<tr>
<td>$V_{TH}$ (V)</td>
<td>0.90</td>
<td>0.10</td>
</tr>
<tr>
<td>$I_{ON}$ [sat, nominal] (mA/µm)</td>
<td>0.45</td>
<td>0.19</td>
</tr>
<tr>
<td>$SS^{-1}$ [nominal] (mV/dec.)</td>
<td>93</td>
<td>86</td>
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Widths from 0.20 to 0.75 µm, respectively. Fig. 8 demonstrates the improvement in knee current (defined as the collector current for a 50% reduction in transistor gain $h_{FE}$) and gate delay of a loaded BiCMOS ring oscillator. The delay in the onset of base push-out or the Kirk effect is predicted theoretically [4] and has been reported in the literature [10]. The thinner epi reduces the component of the collector resistance under the intrinsic device and increases the collector current at the onset of quasi-saturation. Retardation of the onset of base push-out and quasi-saturation both serve to increase the ability of the bipolar

Fig. 5. SEM cross section of a WSi$_3$ polycide emitter n-p-n transistor. The emitter area is $0.8 \times 2.4 \mu m^2$. The polycide is comprised of 2 kÅ WSi$_3$ and 1 kÅ polysilicon.

![SEM cross section of WSi$_3$ polycide emitter n-p-n transistor](image)

Fig. 6. TEM cross section of the emitter polysilicon/silicon interface showing balled up interfacial oxide as well as partial epitaxial regrowth.

![TEM cross section of polysilicon/silicon interface](image)
Fig. 7. Gummel plot for a nominal 
WSi poly emitter n-p-n transistor. 
The emitter area is $0.8 \times 2.4 \mu m^2$. The polycomprise $2 \text{k}\Omega$ WSi, and 
$1 \text{k}\Omega$ polysilicon.

Fig. 8. Measured n-p-n bipolar knee current $I_k$ and loaded BiCMOS gate delay as a function of epitaxial-layer thickness. The knee current is defined 
as the collector current for a 50% reduction in transistor gain.

**TABLE II**

<table>
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<tr>
<th>Parameter</th>
<th>Value</th>
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<tr>
<td>$BV_{CEO}$</td>
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</tr>
<tr>
<td>$BV_{CEO}$</td>
<td>6.5 V</td>
</tr>
<tr>
<td>$BV_{CEO}$</td>
<td>6.0 V</td>
</tr>
<tr>
<td>$C_{EB}$</td>
<td>8 $\text{fF}$</td>
</tr>
<tr>
<td>$C_{CE}$</td>
<td>13 $\text{fF}$</td>
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<tr>
<td>$C_{CS}$</td>
<td>67 $\text{fF}$</td>
</tr>
<tr>
<td>$R_{E}$</td>
<td>25 $\Omega$</td>
</tr>
<tr>
<td>$f_T$</td>
<td>14 GHz</td>
</tr>
<tr>
<td>$h_{FE}$</td>
<td>100</td>
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transistor to source large currents. This combination results in the observed reduction in BiCMOS gate delay. 
Fig. 9 indicates that there is a tradeoff between higher peak cutoff frequency and lower bipolar snapback voltage 
with thinner epitaxial layer thickness. The higher peak cutoff frequency $f_T$ results from the delay in the onset of 
base push-out as well as a narrowing of the intrinsic base. 
The effective collector doping under the base is increased because a constant collector dose has been placed in a 

Fig. 9. Measured n-p-n bipolar snapback voltage $BV_{CEO}$, and peak cutoff frequency $f_T$, as a function of epitaxial layer thickness.

**VI. OPTIMIZATION OF THE SIC IMPLANT**

The selectively ion implanted collector (SIC) [5] has been proposed as a means of increasing cutoff frequency $f_T$ and knee current $I_k$, without sacrificing collector-base capacitance $C_{CB}$. In the SIC approach, an n-type pocket, self-aligned to the emitter, is placed below the active base. 
This pocket cuts off the channeling tail from the boron implant, increasing $f_T$. Additionally, the higher n-type 
doping serves to delay the onset of base push-out or the Kirk effect [4]. The potential benefits of the SIC implant 
were investigated through extensive process and device simulation with PEPPER [6] and MEDUSA [7], respectively. 
Active base and SIC implant conditions were jointly optimized using a matrix of simulations based on an 
experimental design generated by the RS1 software package [8]. Fig. 10 shows simulated doping profiles through the intrinsic bipolar device with and without the SIC implant. Device simulations were performed to study current gain $h_{FE}$, peak cutoff frequency $f_T$, knee current (defined as the collector current for a 50% reduction in $h_{FE}$), $I_k$, and bipolar snapback voltage $BV_{CEO}$, as a function of active base and SIC implant dose and energy. Response surfaces were fitted describing the dependence of these electrical parameters on the implant parameters and contour plots of the results of the device simulations were generated across the matrix of input parameters using RS1. These contour plots are shown in Figs. 11–14. Contour plots of cutoff frequency, knee current, and snapback voltage exhibit clear tradeoffs as implant conditions are varied. The primary dependence for $f_T$ and $I_k$ is on base implant energy. As the base implant energy is reduced, $f_T$ increases while $I_k$ decreases. A narrower base width decreases base transit time and improves peak cutoff frequency. A lower base implant energy results in more
Fig. 10. Simulated doping profiles for the intrinsic bipolar transistor comparing the standard with the SIC devices.

Fig. 11. Contour plots of simulated $f_T$ and $I_C$ characteristics for the nominal n-p-n device as functions of base implant energy and SIC dose. The base implant dose was $2 \times 10^{13}$ cm$^{-2}$ and SIC energy was 150 keV.

Fig. 12. Contour plots of simulated $f_T$ and $I_C$ characteristics for the nominal n-p-n device as functions of base implant energy and SIC implant energy. The base implant dose was $2 \times 10^{13}$ cm$^{-2}$ and SIC implant dose was $3 \times 10^{13}$ cm$^{-2}$.

compensation of the base dopant by the emitter, lowering the peak base doping and lowering the threshold for the onset of high-level injection. Additionally, a shallower base profile implies a larger flat zone which lowers the collector current required for the onset of base push-out or the Kirk effect. Higher SIC doses and lower SIC energies increase $f_T$ by pinching off the base profile and reducing the base width. Higher SIC implant energies and doses improve the knee current by placing more n-type dopant below the intrinsic device and increasing the collector current required for the onset of the Kirk effect. By adjusting the SIC implant dose at fixed active base and SIC implant energies, $I_K$ can be improved by approximately 20% as long as the base implant energy is above 20 keV. A lower SIC implant energy is required to improve $I_K$ for lower energy base implants. Higher SIC implant doses degrade the bipolar snapback voltage because the heavier n-type doping lowers the collector–base breakdown voltage $BV_{CEO}$ and, hence, $BV_{CEO}$. Lower SIC implant energies actually improve $BV_{CEO}$ since more of the SIC implant is compensated by the base profile. Bipolar snapback tends to decrease with lower base implant energies. This correlates with the increase in transistor gain as the base Gummel number is reduced. Simulation
results indicate that an improvement in $I_K$ is expected to be coupled with the reduced $BV_{CEO}$.

The selectively ion implanted collector (SIC) was also investigated experimentally. Fig. 15 is a plot of peak cutoff frequency versus collector current for a series of SIC implant doses. The SIC implant increases $f_T$ from 12 GHz with no implant to a maximum of 19 GHz. Fig. 16 demonstrates that the improved cutoff frequency must be traded off against a lower bipolar snapback voltage $BV_{CEO}$. A peak cutoff frequency of 14 GHz can be achieved while maintaining a $BV_{CEO}$ of 6.5 V.

VII. TUNGSTEN POLYCIDE

The emitter polysilicon layer must be strapped with a silicide to provide a low sheet resistance interconnect for the $V_{SS}$ connection in the bit cell. A WSi$_2$ polycide and a TiSi$_2$ salicide were compared experimentally. The impact of adding a TiSi$_2$ or WSi$_2$ layer on top of the emitter polysilicon was evaluated by examining the n-p-n transistor characteristics as a function of emitter polysilicon thickness and emitter rapid thermal anneal (RTA) sequence.

Formation of a TiSi$_2$ salicide on the emitter polysilicon caused a significant increase in base saturation current ($I_{BSAT}$) and decrease in transistor gain $h_{FE}$ as the emitter polysilicon thickness was decreased. WSi$_2$ polycide only slightly affected the n-p-n characteristics. This is illustrated in Figs. 17 and 18. When the TiSi$_2$ formation is performed prior to the emitter RTA anneal, the structure of the polysilicon emitter is dramatically affected. During salicidation, a large portion of the arsenic implanted into the emitter is lost due to arsenic segregation and consumption during the TiSi$_2$ reaction. This results in a reduction in the arsenic dopant segregated at the polysilicon/silicon interface [9]. The thermal stability of the TiSi$_2$ layer is also an is-
sue. Performing the RTA emitter anneal after formation of the TiSi₂, will often result in agglomeration of TiSi₂. In WSi, polycide devices, some arsenic segregation also occurs, but to a lesser extent. Fig. 19 compares the SIMS profiles for the polysilicon and the WSi, polycide emitter n-p-n transistors. Because of arsenic segregation, the WSi, device has a shallower emitter and thus a wider base and larger base Gummel number. The result is a decrease in transistor gain $h_{FE}$ and emitter resistance $R_E$. The tungsten polycide also exhibited superior thermal stability, exhibiting negligible degradation after the RTA emitter anneal.

VIII. BIPOLAR HCI

It is well known that under reverse-bias emitter–base stress, bipolar transistors undergo HCI (hot carrier injection) degradation which is manifested as an increase in the nonideal base current component and a decrease in the low current gain [11]. Physically, charge is injected into the oxide above the emitter–base junction edge. This results in an increase in the density of interface states (DIT) above the junction edge, which contribute a recombination leakage component to the overall current. In standard operation of a BiCMOS gate, the emitter–base junctions of the bipolar transistors are transiently reverse-biased and bipolar HCI is hence a significant concern. A comprehensive study was carried out of HCI degradation in the bipolar transistors fabricated in this process. Earlier work was confirmed in which the generation of HCI damage is a function of the level of reverse bias stress the device is subjected to. In particular, when bipolar transistors experience a low-level stress corresponding to the band-to-band tunneling region of the reverse emitter–base breakdown characteristic, the nonideal base current component increases as $I^{-1.7}_B \cdot t$, as shown in Fig. 20. When the bipolar transistors are stressed under avalanche breakdown conditions, the nonideal base current component $\Delta I_B$ increases as a function of the total stress charge $Q$. Here, $Q$ is equal to the product of the stress current and total stress time. This is illustrated in Fig. 21. In Fig. 22, the results of bipolar HCI stress under band-to-band tunneling and avalanche breakdown conditions are combined and the time for 50% beta degradation is plotted as a function of reverse stress current for different emitter–base forward biases. It should be noted that the bipolar HCI stressing was carried out under dc conditions whereas the typical emitter–base reverse bias stress a bipolar transistor is subjected to is a transient waveform and the resulting duty cycle is quite low.

IX. ECL RING OSCILLATOR MEASUREMENTS

ECL gate delay was measured as a means of characterizing bipolar performance. Fig. 23 compares gate delay to ECL ring oscillators with single- and double-base n-p-n bipolar transistors laid out with conservative design.
rules and single-base n-p-n bipolar transistors laid out with aggressive design rules. The single-base n-p-n with aggressive design rules achieves an ECL gate delay of 105 ps/gate at a gate current of 350 µA/µm². An ECL ring oscillator with double-base n-p-n bipolar transistors laid out with aggressive design rules would exhibit even faster gate delays. Increased process complexity in the form of a more recessed isolation, a lithographic offset between n⁺ and p⁺ buried layers, and a double-polysilicon, fully self-aligned bipolar structure, would provide improved ring oscillator performance, at the expense of reduced SRAM yield.

The impact of the p⁺ buried layer in increasing the peripheral component of the collector-substrate capacitance $C_{CS}$ was investigated. Fig. 24 demonstrates that leaving out the p⁺ buried-layer implant improves ECL gate delay by approximately 10%. This is at the expense of increasing the minimum n⁻ buried layer to n⁻ buried spacing from 2.5 to 6.5 µm.

X. CONCLUSIONS

A high-performance 0.5-µm BiCMOS technology has been demonstrated which uses a triple-polysilicon process architecture for a fast 4-Mb SRAM class of products. Three layers of polysilicon were used to achieve a compact four transistor bit cell size that is less than 20 µm² by forming self-aligned bit-sense and $V_{th}$ contacts. A WSi₂ polycide emitter n-p-n transistor was implemented with an emitter area of $0.8 \times 2.4 \, \text{µm}^2$ and peak cutoff frequency of 14 GHz. A selectively ion-implanted collector was used to compensate the base channeling tail as well as increase cutoff frequency and knee current while maintaining a collector-to-emitter breakdown voltage of 6.5 V.

n-p-n base and SIC implant conditions were optimized through device simulations coupled with statistical experimental design. A minimum ECL gate delay of 105 ps was achieved at a gate current of 350 µA/µm².

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REFERENCES

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In 1988, he joined Motorola Inc., Austin, TX, as a member of the Advanced Products Research and Development Laboratory. He has since been involved in process integration for 0.5-μm CMOS and BiCMOS fast SRAM’s. His specific projects have included salicide and local interconnect, test vehicle designs for process and device development, and baseline process integration for the 0.5-μm BiCMOS SRAM’s. He is presently Section Manager of the APRDL Diffusion/Epi Process Engineering Group. His current research interests include the application of statistical experimental design techniques to develop and optimize VLSI processes, devices, and circuits.

Dr. Mele is a member of Tau Beta Pi, Eta Kappa Nu, and Phi Kappa Phi.

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In 1969 he joined Texas Instruments to do development for radiation tolerant bipolar and J-FET devices. In 1980 he joined Digital Equipment Corporation where he engaged in CMOS and BiCMOS process development and integration for custom microprocessors. Since 1984 he has been with Motorola working on advanced CMOS and BiCMOS process integration and device engineering projects including nonvolatile and SRAM memory development.

Craig S. Lage received the B.S. degree in physics from the California Institute of Technology, Pasadena, in 1976, and the M.S. degrees in nuclear engineering and electrical engineering from the University of Wisconsin at Madison in 1978 and 1979.

He was employed at Hewlett-Packard in Corvallis, OR, from 1979 until 1985, doing process integration work on CMOS technologies. In 1985 he joined Fairchild Semiconductor in Payzaliah, WA (subsequently acquired by National Semiconductor), where he and his coworkers developed technology used for high-speed BiCMOS 256K and 1-Mb SRAM’s. Since 1990 he has been with Motorola’s Advanced Products Research and Development Laboratory in Austin, TX, working on high-speed BiCMOS SRAM technology.

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