The Sloped-Wall SWAMI—A Defect-Free Zero Bird's-Beak Local Oxidation Process for Scaled VLSI Technology

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***Abstract*—A new scheme for a Side WAll Masked Isolation (SWAMI) process is presented which takes all the advantages provided by LOCOS without suffering its difficulties. The new SWAMI technology incorporates a sloped silicon sidewall and a thin nitride layer around the island sidewalls such that both intrinsic nitride stress and volume expansion-induced stress are greatly reduced. A defect-free fully recessed zero bird's-beak local oxidation process can be realized by the sloped-wall SWAMI. Fabrication technology and NMOS electrical characteristics will be discussed. Two-dimensional simulation of total reduction in effective channel width for ideal vertical isolation, LOCOS, and SWAMI will also be presented. A SWAMI/CMOS circuit including 60K ROM, 2.5K SRAM, and 100 segments of display driver with 5.13 × 5.22 mm^2 chip size has been successfully fabricated. The results indicate that SWAMI is capable of replacing LOCOS as the isolation technology for submicrometer VLSI circuit fabrication.**

I. Introduction

FOR VLSI applications, there is a continual effort in the direction of further reducing device dimensions and, at the same time, increasing the number of devices per single chip. This has imposed stringent requirements on the isolation technology used to separate individual devices in integrated circuits. The basic requirements for VLSI application are: 1) small pattern transfer difference between mask layout dimension and final device geometry, 2) require no scaling down of the field-oxide thickness as other device geometries are scaled down 3) planar surface topology for fine-line lithography, and 4) defect free. It is also desirable that the isolation process is compatible with existing LSI processing techniques and requires no additional photomasking steps. Local oxidation of silicon is a commonly used technology for silicon IC fabrication. However, the so-called bird's beak resulting from LOCOS isolation processing is becoming one of the limiting factors in achieving higher packing density for scaled VLSI. Several approaches have been proposed as an alternative for LOCOS, but either the process introduces defects or the approach requires exotic processing steps which cause other complexities.

A sidewall masked isolation technology (SWAMI) was reported [1] by employing anisotropic silicon and silicon nitride etching to form a bird's-beak free isolation structure. The SWAMI process is compatible with the conventional LOCOS [2] and has a zero bird's beak and a nearly planar surface. However, due to the nature of the vertical sidewalls in the original SWAMI structure, the thickness of the second nitride in the direction perpendicular to substrate is actually very thick. This nitride, around the sidewalls of the island region, forms a rigid film perpendicular to the silicon substrate. It was found [3] that a SWAMI with a vertical sidewall is vulnerable to the formation of dislocations during field oxidation due to volume expansion from oxide intrusion under the second nitride at the foot of island sidewalls. A new SWAMI scheme is presented which takes all the advantages provided by LOCOS without suffering its difficulties. The new SWAMI process incorporates a sloped sidewall and a layer of thin nitride around the island sidewalls such that both intrinsic nitride stress and volume expansion-induced stress are greatly reduced. A defect-free fully recessed zero bird's-beak local oxidation process can be realized by SWAMI.

This paper describes the detailed fabrication process of the sloped-wall SWAMI. A two-dimensional simulation of total reduction in effective channel width for three different isolation structures is discussed. A p-well CMOS circuit including 60K ROM, 2.5K SRAM, and 100 segments of display driver with 5.13 × 5.22 mm^2 chip size fabricated with the SWAMI isolation process is also presented.

The SWAMI Isolation Process

Table I outlines the sequence of steps in the fabrication process used to form the new SWAMI isolation structure. The process is identical to the conventional fully recessed oxidation process except that steps (6) through (10) are added to form this zero bird's-beak and defect-free isolation scheme. In order to avoid the formation of a thick nitride layer perpendicular to the silicon substrate and around the island sidewalls, a C_2F_6 plasma was employed to etch nitride, oxide, and single-crystal silicon in one operation after island patterning. Fig. 1 exhibits the etching characteristics of C_2F_6 plasma. The sloped sidewall on (100) single-crystal silicon can also be obtained by a KOH wet etching. Fig. 2 illustrates schematically the major processing steps of the new SWAMI approach. After island patterning and C_2F_6 plasma etching of nitride/oxide/silicon, channel stop

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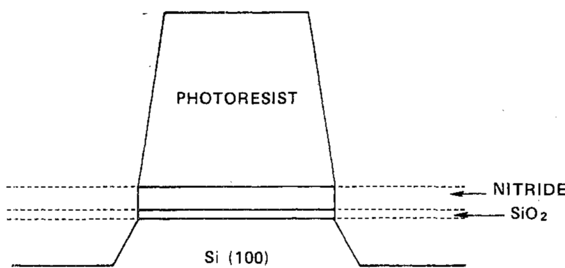
TABLE I

(1) Grow stress relief oxide (SRO I).
(2) Deposit LPCVD nitride (nitride I).
(3) Pattern island region (mask).
(4) Plasma etch nitride I, SRO I, and silicon step.
(5) Channel stop field implant (B+).
* (6) Grow stress relief oxide (SRO II).
* (7) Deposit second nitride (nitride II).
* (8) Deposit LPCVD oxide.
* (9) Plasma etch LPCVD oxide and nitride II in one operation.
*(10) Wet etch LPCVD oxide.
(11) Grow field oxide.
(12) Strip nitrides (chemical).

* Additional processing steps of SWAMI over conventional LOCOS.



C_2F_6 PLASMA ETCH RATE

SiO_2 :	1000Å/min
Si_3N_4 :	1000Å/min
Si (100) :	300Å/min
AZ RESIST:	350Å/min

Fig. 1. C_2F_6 plasma etching characteristics.

boron was implanted. A layer of LPCVD oxide was deposited, as shown in Fig. 2(b), after second stress-relief oxide was grown and the second nitride was deposited. The LPCVD oxide serves as a mask for second nitride etching such that the thin second nitride on the sloped sidewall can be implemented without additional photomasking steps. After anisotropic plasma (C_2F_6) oxide/nitride etching and wet oxide etching to remove the LPCVD oxide ribbon around the island sidewalls, the thin second nitride remains around the sloped sidewall and extends into the planar field regions as shown in Fig. 2(d). During field oxidation, the thin nitride layer on the sloped sidewall will be pushed up due to volume expansion of the field oxide without causing large stress acting on the silicon substrate.

SWAMI provides the flexibility of using relatively thinner nitride and thicker stress-relief oxide such that the intrinsic nitride stress can be drastically reduced. No oxide refill and etch-back are required. Due to the sloped silicon sidewalls, channel stop boron can be implanted onto the silicon sidewalls such that no double threshold voltage effect occurs at the corner of the islands. This double threshold voltage effect occured on an original vertical SWAMI [4]. Fig. 3 shows an SEM cross-sectional view of the isolation structure with SWAMI processing after growth of 640 nm of field oxide at 900°C in steam ambient.

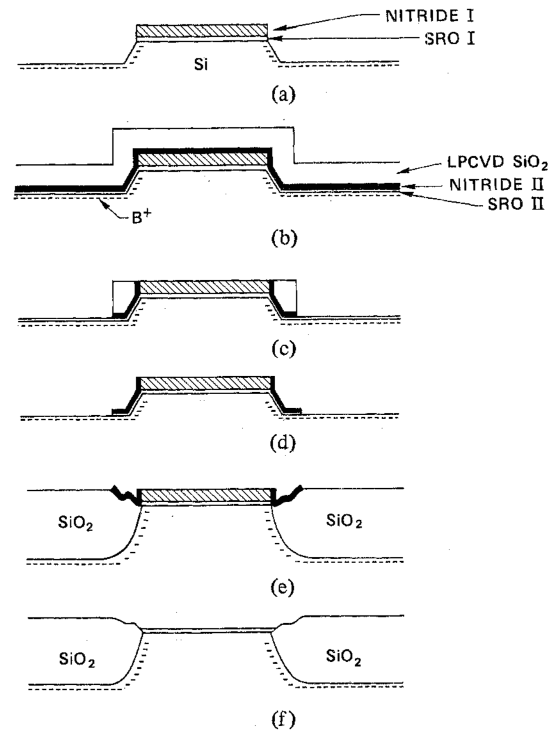


Fig. 2. The major processing steps of the SWAMI: (a) after island patterning and etching; (b) after nitride II and LPCVD oxide deposition; (c) after plasma oxide/nitride etching; (d) island structure before field oxidation; (e) after field oxidation; (f) final isolation structure.

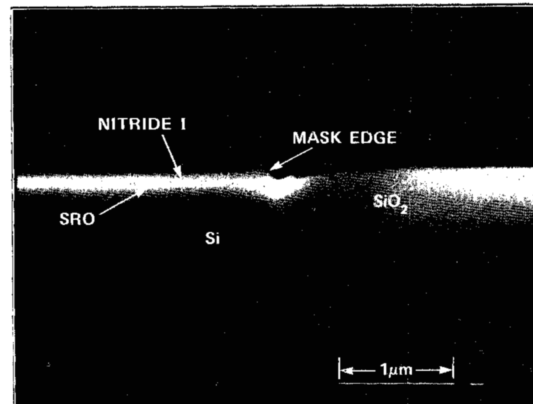


Fig. 3. SEM cross-sectional view of the isolation structure with SWAMI processing after growth of 640-nm field oxide at 900°C.

Fig. 4 reveals the generated dislocations after field oxidation for three different SWAMI approaches. The wafers were decorated by using SECCO etching after field oxides were completely removed. With thick nitride around vertical sidewalls, defects are generated at the corners of the patterned islands due to the tensile stress of the thick nitride. With thin nitride around the vertical sidewalls, defects are generated over the entire edges due to volume expansion of the intruded oxide under the second nitride around the island sidewalls [3]. The number of defects due to this mechanism depends on the field oxide thickness and oxidation temperature. With sloped sidewall and thin second nitride, a defect-free zero bird's-beak local oxidation process can be realized by SWAMI.

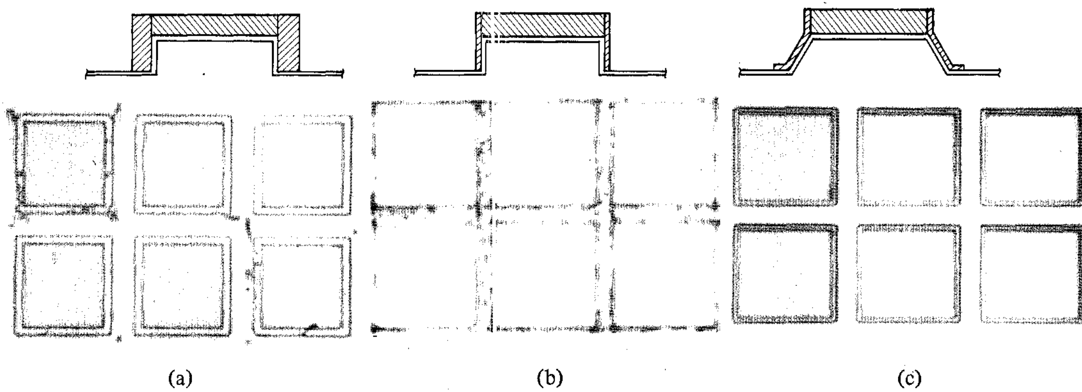


Fig. 4. Comparison of oxidation-induced defects for three different SWAMI approaches. (a) Vertical sidewalls with thick nitride II. (b) Verical sidewalls with thin nitride II. (c) Sloped sidewall with thin nitride II.

TABLE II

Field oxide	:	700 nm
Gate oxide	:	25 nm
Field implant	:	B+, 70 Kev, 3E12/cm2
Cnannel implant	:	B+, 50 Kev, 9E11/cm2
Gate electrode	:	N+ polysilicon, 350 nm
Source/drain junction depth	:	250 nm

Device Characteristics

After the SWAMI isolation structure was formed, an NMOS polysilicon gate process was employed to fabricate MOSFET's. Process parameters are listed in Table II. After MOSFET devices are fabricated, the temperature-bias stressed *C-V* and breakdown voltage of gate oxide capacitors were measured to investigate the integrity of the final gate oxide in terms of its stability of the interface charges, the breakdown field, and the defect density of the thin gate oxide. Test capacitor structure was designed with very long island edges to investigate the effect of island sidewalls on the integrity of gate oxide. Test results indicate that both fixed charge and mobile charge densities are approximately at $3E10/cm^2$. The histogram of the measured gate breakdown voltage is shown in Fig. 5. The 25-nm gate oxide with the SWAMI isolation process has a defect density below 10 $defects/cm^2$.

As mentioned earlier, defect generation during field oxidation is one of the major concerns of the sidewall masked isolation process. The defects, usually edge dislocations, are likely to cause higher diode junction leakage by providing deep recombination centers especially by attracting heavy metal impurities. Therefore, it is important to measure the leakage current of diodes fabricated with the SWAMI process and compare it with diodes fabricated with the LOCOS process. Fig. 6 shows the diode leakage current as a function of junction temperature for three different kinds of diodes. The finger diode has the same planar area as the planar diode except that the total length of island edges is more than 10 times longer. As discussed previously, if there are any extra defects generated from the SWAMI process, they will be generated along the island edges. Since a

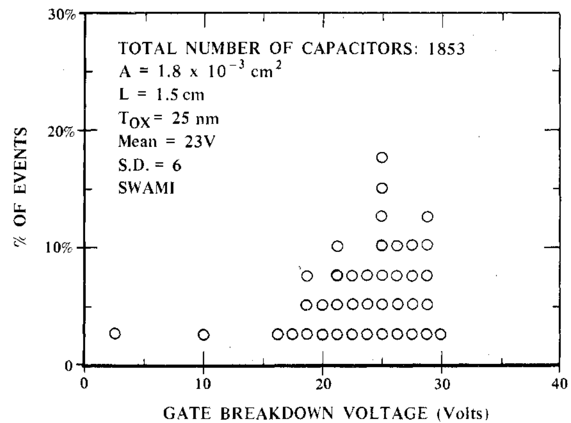


Fig. 5. Histogram of gate oxide breakdown voltage for gate capacitors processed with the SWAMI.

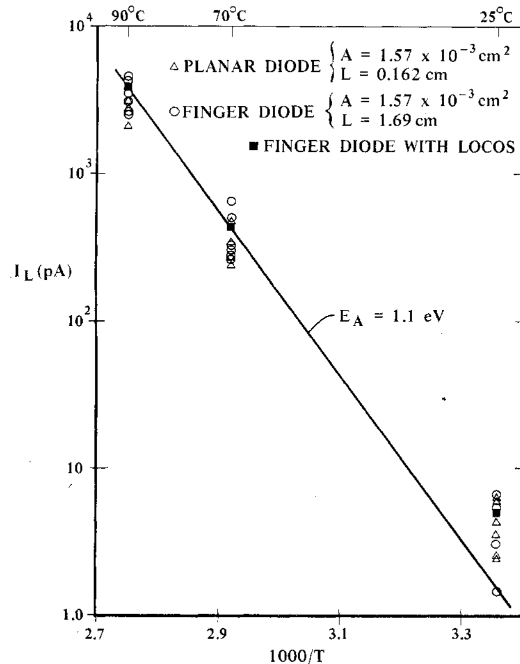


Fig. 6. Diode leakage current as a function of junction temperature.

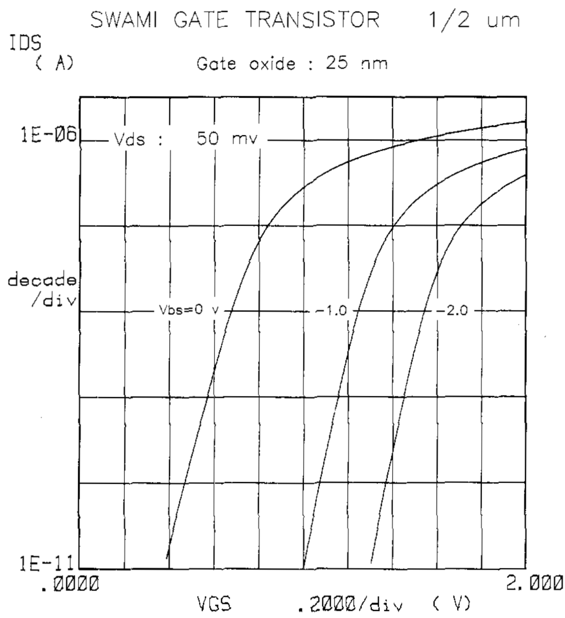


Fig. 7. Measurement of turn-on characteristics of enhancement gate transistor with W/L (mask) = 1/2 μm. T(field oxide) = 700 nm, and T(gate oxide) = 25 nm.

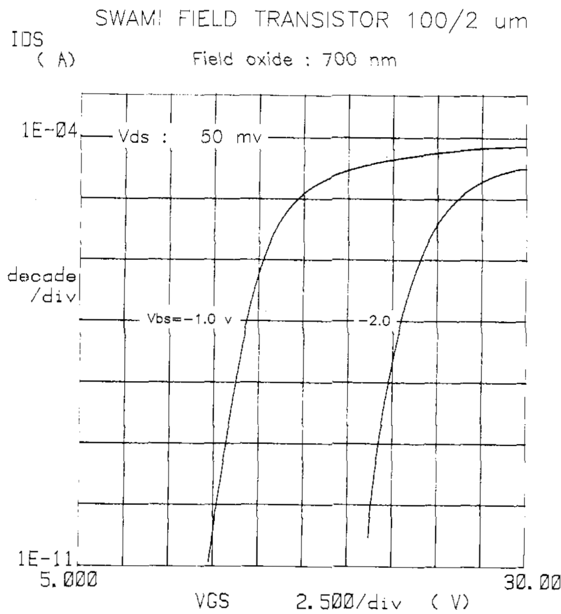


Fig. 8. Measurement of turn-off behavior of polysilicon-gated parasitic field transistor with island spacing of 2 μm.

finger diode has longer island edges, it will have a higher leakage current than the planar diode. Diodes fabricated with SWAMI will have a higher leakage current than diodes fabricated with LOCOS. Test results indicate that almost all three different diodes have identical leakage current with activation energy of 1.1 eV, which is the diffusion-limited leakage current. The diode leakage-current measurement confirms that the SWAMI process does not generate any extra defects as compared to the LOCOS process.

Measurements of the turn-on behavior of a gate transistor with mask layout dimensions of W/L = 1/2 μm are shown in Fig. 7.

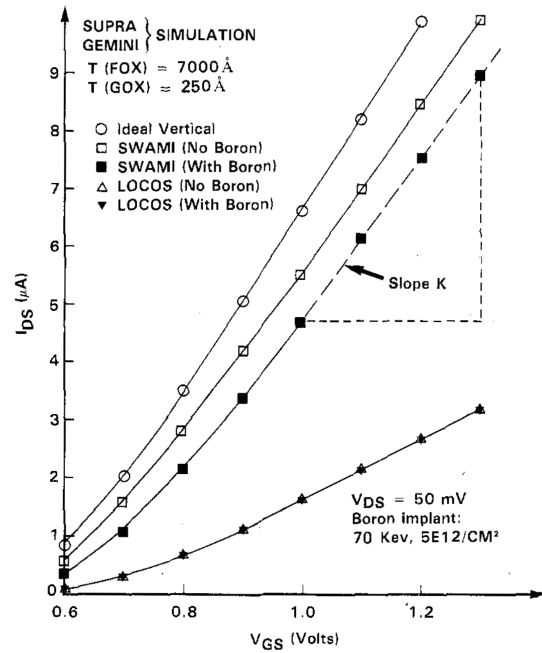


Fig. 9. Two-dimensional simulated I-V characteristics of enhancement gate transistor with W(mask) = 2 μm, and L(effective) = 1 μm.

No double threshold voltage occurs in subthreshold characteristics. The subthreshold slope obtained from gate transistors is approximately 80 mV/decade. The turn-off characteristics of a polysilicon-gated parasitic field oxide device with a layout spacing of 2 μm is shown in Fig. 8. The turn-off rate of the field transistors is about 500 mV/decade. There is little difference in the transistor turn on/off behavior for devices fabricated with SWAMI or with LOCOS. Due to its steeper oxide-to-silicon isolation boundary and the fully recessed isolation structure, the SWAMI devices have a better narrow-width effect [5].

Two-Dimensional Device Simulation

SWAMI completely eliminates the lateral oxidation of LOCOS. However, the reduction in effective channel width from mask layout width can still come from boron encroachment due to the channel stop boron implant for n-channel devices. In order to quantitatively predict the ΔW of the SWAMI process, two-dimensional simulation has been performed to compare the total reduction in effective channel width for ideal vertical isolation, LOCOS, and SWAMI. The isolation structures were simulated by using the SUPRA [6] program. The current-voltage characteristics (I_{ds}-V_{gs}) of a device with a mask drawn width of 2 μm and an effective channel length of 1 μm was calculated using the GEMINI [7] program, with the device biased in the linear region. The total effective channel width narrowing can be measured from the slope K of the I_{ds}-V_{gs} curve, which is proportional to the effective width of the transistor. The value of K was calculated for the preceding three isolation structures. The device has a gate oxide thickness of 25 nm and an intrinsic mobility of 600 $cm^2/V \cdot s$. ΔW due to boron encroachment is studied by comparing device characteristics for the case with a 70-KeV boron implant at a dose of $5E12/cm^2$ and the case without a field boron implant. Fig. 9 shows the calculated I-V characteristics for a field oxide thickness of 700 nm.

TABLE III
GEMINI SIMULATION OF ΔW FOR IDEAL VERTICAL ISOLATION, SWAMI, AND LOCOS

Isolation	K (μA/V)		K/K* (ideal)		W_{eff} (μm)		ΔW (μm)	
Structure	5000 Å	7000 Å	5000 Å	7000 Å	5000 Å	7000 Å	5000 Å	7000 Å
Ideal Vertical	16.14	16.16	1.0	1.0	2.0	2.0	0	0
LOCOS (no B+)	10.05	5.272	0.622	0.326	1.245	0.653	0.378	0.670
LOCOS (with B+)	9.96	5.263	0.617	0.326	1.234	0.652	0.383	0.670
SWAMI (no B+)	14.37	14.40	0.890	0.892	1.780	1.783	0.110	0.108
SWAMI (with B+)	14.10	14.09	0873	0.872	1.746	1.745	0.127	0.128

K*: K value for ideal vertical isolation (= 16.15 μA/V)

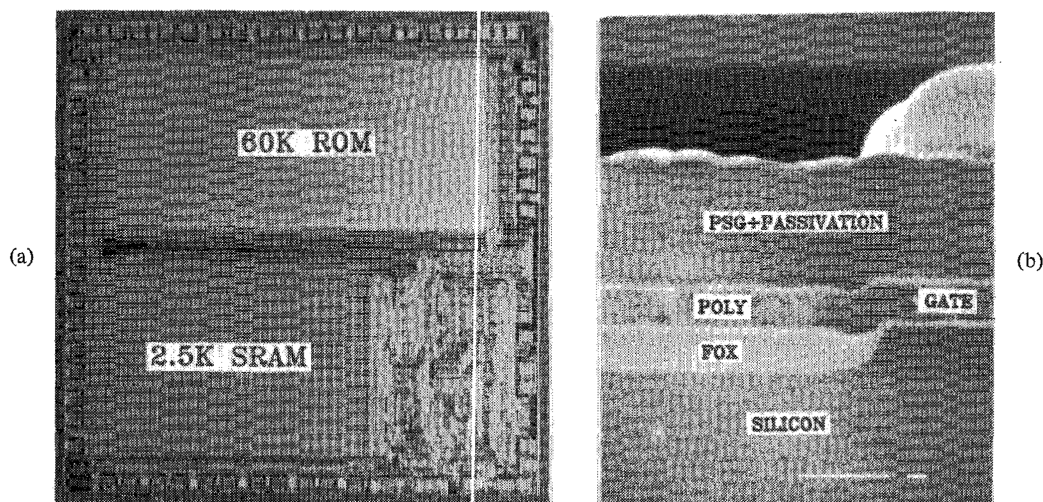


Fig. 10. (a) Photomicrograph of p-well CMOS circuit processed with the SWAMI. This circuit containing 60K ROM, 2.5K SRAM, and 100 segments of display driver. Chip size is 5.13 × 5.22 mm^2. (b) SEM cross-sectional view of device structure with SWAMI processing. T(poly) = 500 nm, T(field oxide) = 600 nm, and T(gate oxide) = 50 nm.

Table III shows the value of K for three different isolation structures. Two field oxide thicknesses, 500 and 700 nm, were considered in this study. The effective channel width and hence ΔW can be calculated by comparing the value of K to the ideal vertical isolation. In the case of LOCOS, ΔW comes mainly from oxide encroachment which is about 90 percent of field oxide thickness. With no channel-stop boron implant, the SWAMI process produces a loss of effective channel width of approximately 0.1 μm regardless of field-oxide thickness. This ΔW result from the SWAMI process is due to the sloped silicon sidewall etch before field oxidation. With KOH silicon step etching, ΔW in SWAMI can be reduced to boron encroachment only. When the field boron implant and following thermal cycles are considered, the SWAMI process showed about 0.02 μm of boron encroachment while LOCOS showed almost negligible boron encroachment at 900°C oxidation. As it shown in Fig. 9, the boron encroachment also produces a slightly higher device threshold voltage in the case of the SWAMI process which can be compensated for by reducing the channel implant dose.

The feasibility of the SWAMI isolation process for VLSI circuit fabrication has been successfully verified by fabricating a p-well CMOS circuit. This CMOS circuit, as shown in Fig. 10(a), contains 60K ROM, 2.5K SRAM, and 100 segments of display driver with a 5.13 × 5.22 mm^2 chip size. Fig. 10(b) illustrates the cross-sectional view of the device structure in this circuit. It shows the improvement in surface planarity over devices fabricated with LOCOS. Indentical production yield for circuits processed with SWAMI and with conventional LOCOS has been achieved. This result demonstrates that the sloped-wall SWAMI process is suitable for the VLSI production environment. Since the minimum feature size of this production circuit is 4 μm, improvement in circuit performance from the SWAMI process is not observed. However, as feature sizes are scaling down to below the 1-μm level, significant enhancement in circuit performance can be expected.

CONCLUSIONS

A defect-free fully recessed zero bird's-beak local oxidation process can be achieved by SWAMI. This new isolation process features: defect-free, planar surface topology, no additional masking step is required, and its process is compatible with existing LSI processing techniques. It offers several advantages over conventional LOCOS processing such as: 1) zero bird's beak, 2) no scale down of field-oxide thickness is required as other device geometries are scaled down, and 3) planar surface topology. SWAMI fullfills all the requirements needed for submicrometer VLSI circuit fabrication. In addition, its unique isolation structure provides several novel applications for advanced CMOS technology [5].

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Selective Low-Pressure Silicon Epitaxy for MOS and Bipolar Transistor Application

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***Abstract*—The selective low-pressure epitaxy is presented in this paper. In contrast to LOCOS technology, this process starts with structuring a thick field oxide by anisotropic RIE etching. Then monocrystalline silicon is grown selectively in the windows formed. Si-gate MOS transistors have been produced using this technology.**

In the field of bipolar transistors, reactive ion etching and selective low-pressure epitaxy has been used to optimize the Schottky collector transistor to a nearly one-dimensional structure. These transistors have been built on a submicrometer epitaxial layer.

INTRODUCTION

ONE OF THE major concerns in further increasing the packing density of VLSI circuits is device isolation. Until now, LOCOS (Fig. 1) has been used most frequently in VLSI technology. However, further decreasing the feature size of devices leads to drawbacks in the device characteristics. Among these are the bird's beak, which reduces the active area and results in a nonplanar surface; the white-ribbon effect; and the outdiffusion of the channel stopper into the active device area, which increases the sidewall capacity, reduces the breakdown voltage, and produces a narrow-channel effect [1]. All these reasons have led to intensive research work with a view of finding a new dielectric device-isolation technique [2]-[6].

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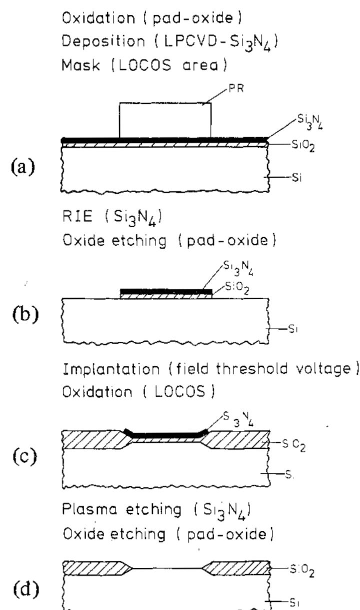

Fig. 1. LOCOS process sequence.

An alternative to LOCOS technology which avoids the drawbacks mentioned earlier is selective epitaxy.

PROCESS SEQUENCE

The process sequence for this new technology is shown in Fig. 2. Processing of the wafer starts with oxidation. The oxide obtained is to serve as field oxide for device isolation.

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