THE SWAMI - A DEFECT FREE AND NEAR-ZERO BIRD's-BEAK LOCAL OXIDATION PROCESS AND ITS APPLICATION IN VLSI TECHNOLOGY

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ABSTRACT

A new scheme for SWAMI (Side WAll Masked Isolation) process is presented which takes full advantage of LOCOS processing without suffering the difficulties. The new SWAMI technology incorporates a sloped silicon sidewall and thin nitride around the island sidewalls such that both intrinsic nitride stress and volume expansion induced stress are greatly reduced. A defect free and near-zero bird's beak local oxidation process can be realized by the SWAMI. Fabrication technology and MOSFET electrical characteristics will be discussed. A SWAMI/CMOS circuit including 60K ROM, 2.5K SRAM, and 100 segments of display driver with 5.13 x 5.22 mm2 chip size has been successfully fabricated. The results indicate that the SWAMI is capable of replacing the LOCOS as the isolation technology for scaled VLSI circuit fabrication.

INTRODUCTION

As device geometries are scaled down to the micrometer and submicrometer range, a new isolation technology to provide the smallest pattern transfer difference between mask and active device geometry for any giving lithographic technique is required. It is desirable that the new isolation technology have the following properties: 1) defect free; 2) require no scaling down of the field oxide thickness as other geometries are scaled down; 3) planar surface; 4) require no additional photomasking steps; and 5) compatible with existing LSI processing techniques.

A sidewall masked isolation technology (SWAMI) was reported [1] by employing anisotropic silicon and silicon nitride etching to form a bird's-beak free isolation structure. The SWAMI process is compatible with the conventional LOCOS [2] and has a zero bird's-beak and a nearly planar surface. However, due to the nature of the vertical sidewalls in the original SWAMI structure, the thickness of the second nitride in the direction perpendicular to substrate is actually very thick. This nitride, around the sidewalls of the island region, forms a rigid film perpendicular to the silicon substrate. It was found [3] that the original SWAMI is vulnerable to the formation of dislocations during field oxidation due to volume expansion from oxide intrusion under the second nitride at the foot of island sidewalls. A new SWAMI scheme is presented which takes full advantage of LOCOS processing without suffering the difficulties. The modified SWAMI process incorporates a sloped sidewall and a layer of thin nitride ($\sim$ 300A) around the island sidewalls such that both intrinsic nitride stress and volume expansion induced stress are greatly reduced. A defect free and near-zero bird's-beak local oxidation process, with more than 70% of the field oxide recessed below the silicon active regions, can be realized by the SWAMI.

This paper describes the new SWAMI fabrication process, the device electrical characteristics, and its impact on scaled VLSI technology. A P-well CMOS circuit including 60K ROM, 2.5K SRAM, and 100 segments of display driver with 5.13 x 5.22 mm2 chip size fabricated with the SWAMI isolation process is also presented.

The SWAMI Isolation Process

Table I outlines the sequence of steps in the fabrication process to form the new SWAMI isolation structure. The process is identical to the conventional fully-recessed oxidation process except that steps (6) through (10) are added to form this near-zero bird's-beak and defect free isolation scheme. In order to avoid the formation of a thick nitride layer perpendicular to the silicon substrate and around the island sidewalls, a C_2F_6 plasma was employed to etch nitride, oxide, and single crystal silicon in one operation after island patterning. Figure 1 exhibits the etching characteristics of C_2F_6 plasma. The sloped sidewall on (100) single crystal silicon can also be obtained by a KOH wet etching. Figure 2 illustrates schematically the major processing steps of the new SWAMI approach. After island patterning and C_2F_6 plasma etching of nitride/oxide/silicon, channel stop boron was implanted. A layer of LPCVD oxide was deposited, as shown in Figure 2(b), after second stress relief oxide was grown and the second nitride was deposited. The LPCVD oxide serves as a mask for second nitride etching such that thin second nitride on sloped sidewall can be implemented without additional photomasking steps. After anisotropic plasma (C_2F_6) oxide/nitride etching and wet oxide etching to remove the LPCVD oxide ribbon around the island sidewalls, the thin second nitride remains around the sloped sidewall and extends into the planar field regions as shown in Figure 2(d). During field oxidation,

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CH1832-5/82/0000-0224 $00.75 © 1982 IEEE

the thin nitride layer on the sloped sidewall will be pushed up due to volume expansion of the oxide without causing large stress acting on the silicon substrate.

The new SWAMI provides the flexibility of using relatively thinner nitride and thicker stress relief oxide such that the intrinsic nitride stress can be drastically reduced. No oxide re-fill and etch-back are required. Due to the sloped silicon sidewalls, channel stop boron can be implanted onto the silicon sidewalls such that no double threshold voltage effect occurs at the corner of the islands [4,5]. Figure 3 shows an SEM cross-sectional view of the isolation structure with SWAMI processing after growth of 640 nm of field oxide at 900 °C in steam ambient. The length of the bird's-beak can be controlled to less than 0.1 um for a field oxide thickness thicker than 0.8 um, and more than 70% of the field oxide is recessed below island surface.

Device Characteristics

After the SWAMI isolation structure was formed, an NMOS polysilicon gate process was employed to fabricate MOSFET's. Process parameters are listed in Table II. After MOSFET devices are fabricated, temperature-bias stressed C-V and breakdown voltage of gate oxide capacitors were measured to investigate the integrity of the final gate oxide in terms of its stability of the interface charges, the breakdown field, and the defect density of the thin gate oxide. Test capacitor structure was designed with very long island edges to investigate the effect of island sidewalls on the integrity of gate oxide. Test results indicate that both fixed charge and mobile charge densities are approximately at 3E10/cm2. The histogram of the measured gate breakdown voltage is shown in Figure 4. The 25 nm gate oxide with the SWAMI isolation process has defect density below 10 defects/cm2.

As mentioned earlier, defect generation during field oxidation is one of the major concerns of the sidewall masked isolation process. The defects, usually edge dislocations, are likely to cause higher diode junction leakage by providing deep recombination centers especially by attracting heavy metal impurities. Therefore, it is important to measure leakage current of diodes fabricated with the SWAMI process and compare it with diodes fabricated with the LOCOS process. Figure 5 shows the diode leakage current as a function of junction temperature for three different kinds of diodes. The finger diode has the same planar area as the planar diode except that the total length of the island edges is more than 10 times longer. As discussed previously, if there are any extra defects generated from the SWAMI process they will be generated along the island edges. Since finger diode has longer island edges, it will have higher leakage current than the planar diode and diodes fabricated with the SWAMI will have higher leakage current than diodes fabricated with the LOCOS. Test results indicate that almost all three different diodes have identical leakage current with activation energy of 1.1 ev, which is the diffusion limited leakage current. The diode leakage current measurement confirms that the SWAMI process does not generate any extra defects as compared to the LOCOS process.

Measurements of turn-on behavior of gate transistor with mask layout dimensions of W/L=1/2 um is shown in Figure 6. No double threshold voltage occurs in this subthreshold curve. The subthreshold slope obtained from this transistor is approximately 80 mv/decade. The turn off characteristics of polysilicon-gated parasitic field oxide device with layout spacing of 2 microns is shown in Figure 7. The turn-off rate of field transistor is about 550 mv/decade. There is little difference in transistor turn on/off behavior for devices fabricated with the SWAMI or with the LOCOS process.

The feasibility of the SWAMI isolation process for VLSI circuit fabrication has been successfully verified by fabricating a P-well CMOS circuit with reasonable yield. This CMOS circuit, as shown in Figure 8(a), contains 60K ROM, 2.5K SRAM, and 100 segments of display driver with 5.13 x 5.22 mm2 chip size. Figure 8(b) illustrates the cross-sectional view of the device structure in this circuit. It shows the improvement in surface planarity over devices fabricated with the LOCOS.

CONCLUSION

A defect free and near-zero bird's-beak local oxidation process has been successfully demonstrated by the SWAMI. This new isolation process features: defect free, simple process, planar surface topology, no additional masking step is required, and its process is compatible with existing LSI processing techniques. It offers several advantages over the conventional LOCOS processing such as: (a) near-zero bird's-beak; (b) no scale down of field oxide thickness is required as other device geometries are scaled down, and (c) planar surface topology. These advantages not only enhance VLSI circuit performance and packing density, but also improve the production yield especially when device feature size is shrinking down below one-micron level.

ACKNOWLEDGMENT

The authors would like to thank the entire staff of HP IC Processing Laboratory for processing the wafers. Thanks are due to Fred Schwettmann and Bob Grimm for their support and encouragement during the course of this work.

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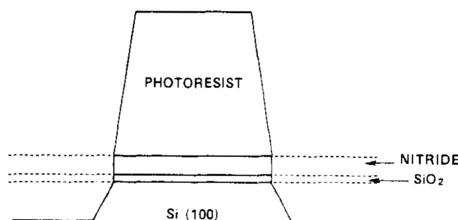
Table I. Sequence of processing steps in SWAMI approach

(1) Grow stress relief oxide (SRO I)
(2) Deposit LPCVD nitride (nitride I)
(3) Pattern island region (mask I)
(4) Plasma etch nitride I, SRO I, and silicon step (in one operation)
(5) Channel stop field implant (B+)
(6) Grow stress relief oxide (SRO II)
(7) Deposit second nitride (nitride II)
(8) Deposit LPCVD oxide
(9) Plasma etch LPCVD oxide and second nitride in one operation (no mask)
(10) Wet etch LPCVD oxide
(11) Grow field oxide
(12) Strip nitrides (chemical)



C_2F_6 PLASMA ETCH RATE

SiO_2 :	1000Å/min
Si_3N_4 :	1000Å/min
Si (100) :	300Å/min
AZ RESIST:	350Å/min

Fig.1. C2F6 plasma etching characteristics.

Table II. Process parameters of NMOS/SWAMI devices

Field oxide	**: 700 nm**
Gate oxide	**: 25 nm**
Field implant	**: B+, 70Kev, 3E12/cm2**
Channel implant	**: B+, 50Kev, 9E11/cm2**
Gate electrode	**: N+, 350 nm**
S/D junction	**: 250 nm**

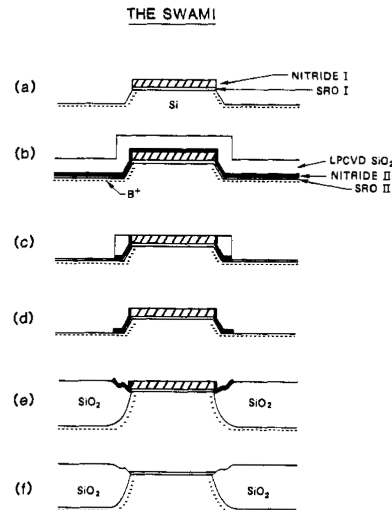


Fig.2. The major processing steps of the SWAMI.
(a). After island patterning and etching.
(b). After nitride II and LPCVD oxide deposition.
(c). After plasma oxide/nitride etching.
(d). Island structure before field oxidation.
(e). After field oxidation.
(f). Final isolation structure.

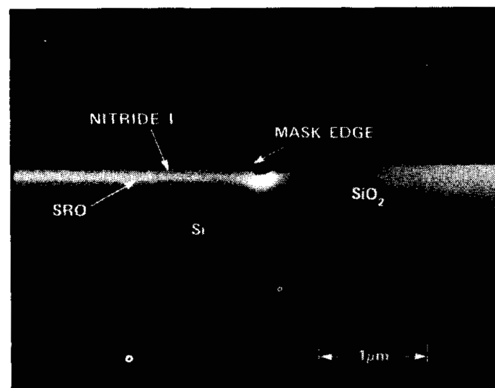


Fig.3. SEM cross-sectional view of the isolation structure with SWAMI processing. T(FOX)=6400 A. T(nitride I)=1200 A. T(nitride II)=300 A. T(SRO I)=500 A. T(SRO II)=150 A.

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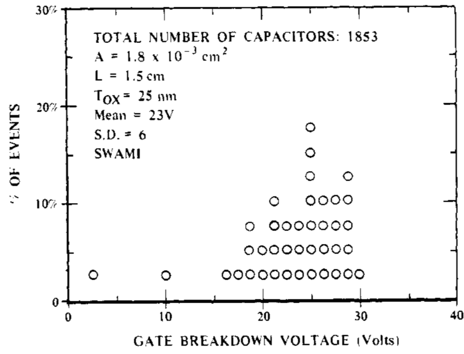


Fig.4. Histogram of gate oxide breakdown voltage.

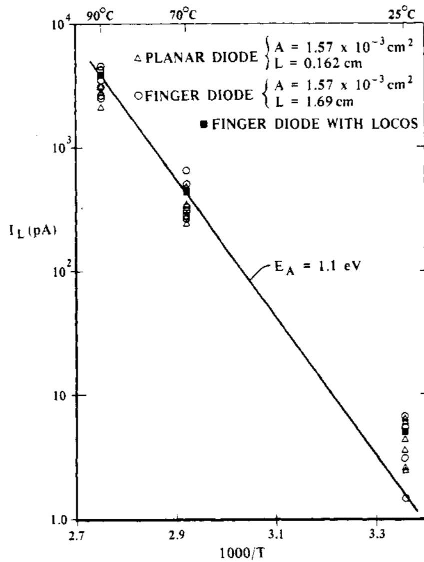
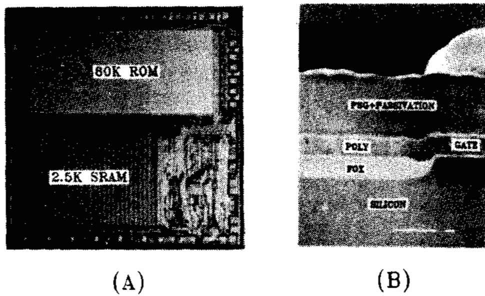


Fig.5. Diode leakage current versus junction temperature.



(A) (B)

Fig.8. (A). Photomicrograph of CMOS circuit containing 60K ROM, 2.5K SRAM, and 100 segments of display driver. Chip size is 5.13 * 5.22 mm2.

(B). SEM cross-sectional view of device structure with SWAMI processing. T(poly)= 500 nm, T(Fox)=600nm,and T(Gox)=50nm.

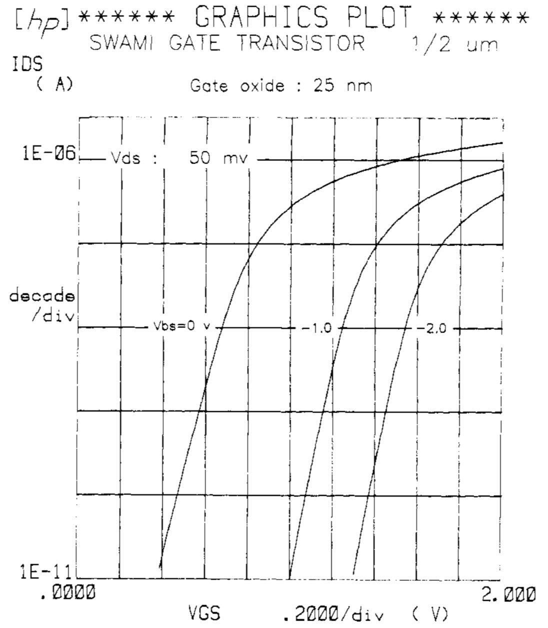


Fig.6. Subthreshold curve of enhancement gate transistor. T(FOX)=7000 A, T(GOX)=250 A.

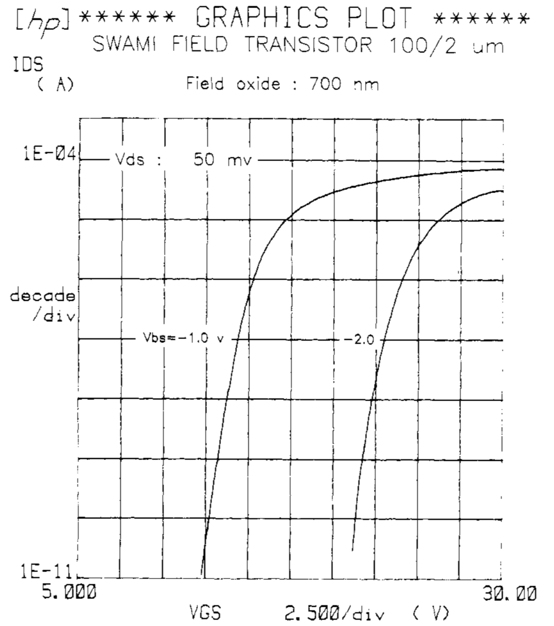


Fig.7. Turn-off behavior of parasitic field transistor.

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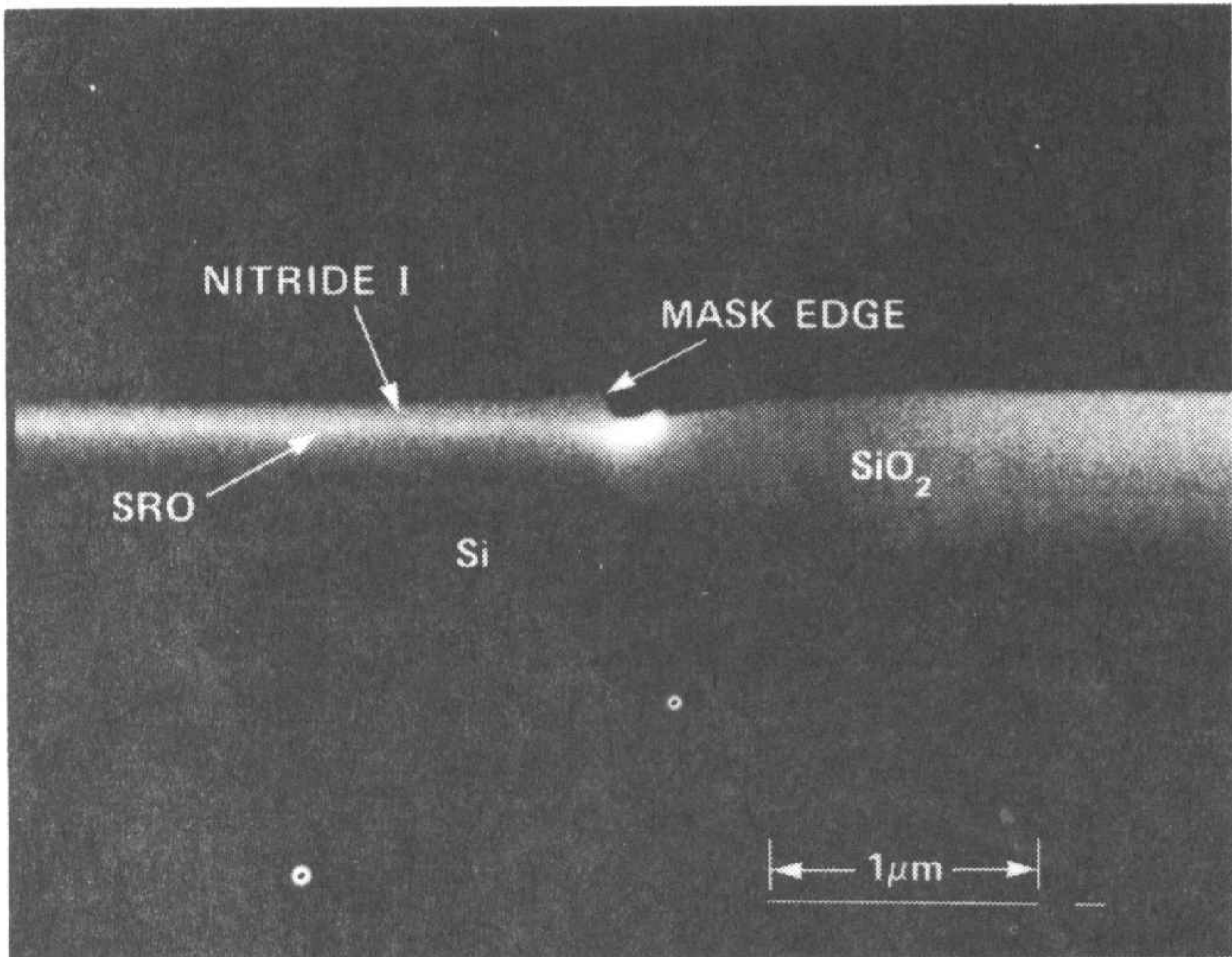

Fig.3. SEM cross-sectional view of the isolation structure with SWAMI processing. T(FOX)=6400 A. T(nitride I)=1200 A. T(nitride II)=300 A. T(SRO I)=500 A. T(SRO II)=150 A.