Soft-Error-Rate Improvement in Advanced BiCMOS SRAMs

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Abstract

A dramatic improvement in soft-error-rate (SER) is achieved by implementing a triple-well structure in a BiCMOS process. For 4Mb SRAMs fabricated in a BiCMOS process, an optimized triple-well process improves the accelerated SER (ASER) by over two orders of magnitude without compromising device performance. Diode charge collection and ASER measurements show excellent correlation across several BiCMOS and CMOS processes.

Introduction

Alpha-particle-induced soft errors are one of the primary reliability concerns in advanced memory circuits [1-9]. Device scaling necessitates smaller devices and parasitic capacitances, resulting in smaller stored charge in the SRAM cell which increases the likelihood of soft errors. Additionally, many high-speed, high-density SRAM memories employ a BiCMOS process to provide the necessary product requirements [10]. To provide isolation of the bipolar collector devices, the BiCMOS substrate is p-type. With self-aligned twin wells on the p-sub, the SRAM cells are in a p-well with the p-sub underneath. It has been shown from CMOS processes that the p-well/p-sub structure is much worse for SER than a p-well/n-sub structure [3,8]. The potential barrier at the p-well/n-sub junction reduces the collection of electrons generated in the silicon by the alpha particle. This paper describes the application of a highly doped p+ buried layer and of a triple-well structure to reduce the soft-error-rate (SER) in a 4Mb BiCMOS SRAM process. For the highly doped p+ buried layer, SER is reduced by an order of magnitude, while for the optimized triple-well structure, SER is reduced by over two orders of magnitude. For the first time, diode charge-collection and SRAM accelerated SER measurements are correlated across several processes.

SER Measurements

Figure 1 shows the charge-collection spectra of a 64K array of memory cell active areas inside a p-well measured using a thorium foil [5]. The charge-collection measurements were performed on arrays made with standard 0.5 µm CMOS and BiCMOS processes [10], an elevated p+ buried layer process ("P+BL"), and two

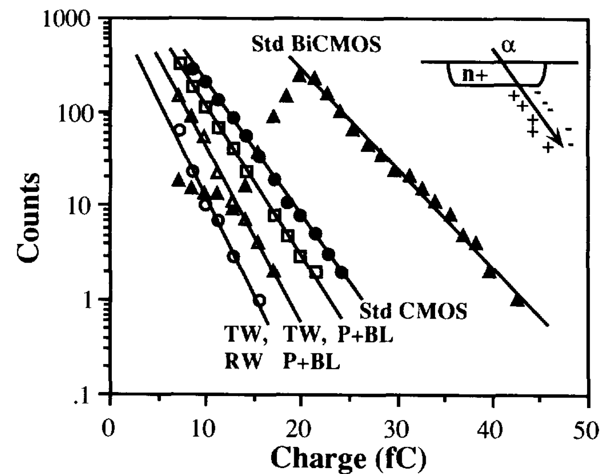

Figure 1. Charge collection spectra for the different processes taken from a 64k array of active areas (Vn+ = 5V).

different triple-well processes ("TW,P+BL" and "TW,RW"). An exponential tail for each distribution is observed, as shown in Figure 1. The lower range of charge collected is limited by the measurement set-up. The standard BiCMOS process has higher collected charge compared to the other processes, with the triple-well processes providing the lowest charge collection.

Accelerated soft-error-rate (ASER) was also measured on 4Mb SRAMs made with these different processes (Figure 2). In general, the ASER results agree well with the charge collection measurements as the standard BiCMOS process shows the highest SER and the triple-well processes show the lowest SER. At 5V operation, as projected from the data in Figure 2, a standard BiCMOS process exhibits ~7X higher SER than a standard CMOS process. Because the two p-wells have similar doping, this difference is attributed to the p-well/n-sub junction under the array for the CMOS process, while the BiCMOS process does not have another junction under the array (p-well/p-sub). This factor could be larger if the BiCMOS process did not include a p+ buried layer which reduces the charge collection [5]. Elevating the p+ buried layer dose reduces the SER to about the same as the standard CMOS process, providing a SER improvement of ~8X over the standard BiCMOS process. The best improvement in SER is achieved with

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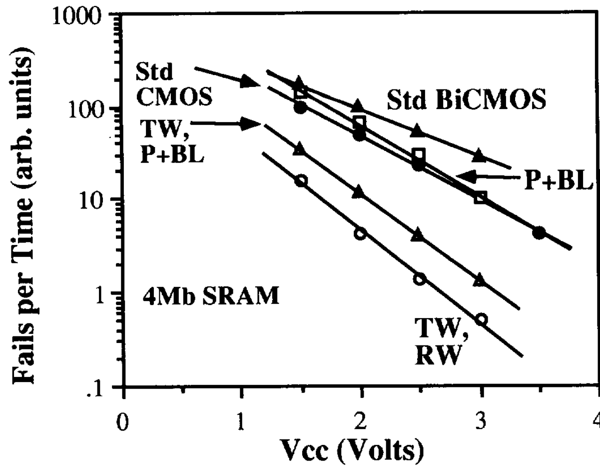

Figure 2. Accelerated soft-error rate (ASER) of 4Mb SRAMs.

the triple-well processes, in which SER reductions of 150X and 600X are realized.

From the charge collection measurements in Figure 1, the probability of a charge transfer greater than Q_{CRIT}, the charge needed to create an upset, equals the number of counts greater than Q_{CRIT} divided by the total number of counts [3,11,12] and is noted here by $P(Q>Q_{CRIT})$. Because the soft error rate is proportional to $P(Q>Q_{CRIT})$ [11,12], the measurements in Figure 2 should correlate with $P(Q>Q_{CRIT})$ calculated from Figure 1. This relationship between charge collection and ASER data is established in Figure 3, in which the critical charge for generating a soft-error at 5V is 20 fC. This is the first time that the charge collection and ASER measurements have been correlated in this fashion across several processes. All of the processes fit the curve in Figure 3 well except for the standard BiCMOS process. The high value of $P(Q>Q_{CRIT})$ for this process is believed to occur because the array for the charge collection measurements has all of the active nodes connected together. Because of the lighter doping and lack of a p/n junction under the p-well, the standard BiCMOS process has a large amount of diffusion charge collected by surrounding nodes [13] which creates an arithmetic offset in the charge axis.

With the exponential tails for the charge collection distributions shown in Figure 1, $P(Q>Q_{CRIT})$ is exponentially dependent on Q_{CRIT}

$$P(Q>Q_{CRIT}) \propto \int_{Q_{CRIT}}^{\infty} N(Q)dQ \propto 10^{-BQ_{CRIT}} \qquad (1)$$

where B is the slope of a given distribution, N(Q), in Figure 1. Because the soft error rate, E_R, is proportional to P(Q) [11,12], the slope of the curves in Figure 2 is expressed as

$$\frac{\partial(\log E_R)}{\partial V_{CC}} = -B\frac{\partial Q_{CRIT}}{\partial V_{CC}} \qquad (2).$$

This predicts that the slope of the ASER versus V_{CC} curves in Figure 2 should equal the slope of the charge collection distributions in Figure 1 times the Q_{CRIT} dependence on V_{CC}. Simulations of Q_{CRIT} as a function of V_{CC}, done in a similar fashion as [8], show a linear fit with a slope of 5 fC/V, which agrees well with a measured node capacitance of 5.9 fF. Figure 4 shows that the slopes of the distributions of Figures 1 and 2 correlate well with a dependence of 5 fC/V, in excellent agreement with the Q_{CRIT} simulation. This is the first time that the V_{CC} dependence of the ASER has been correlated with the charge collection distributions in this fashion.

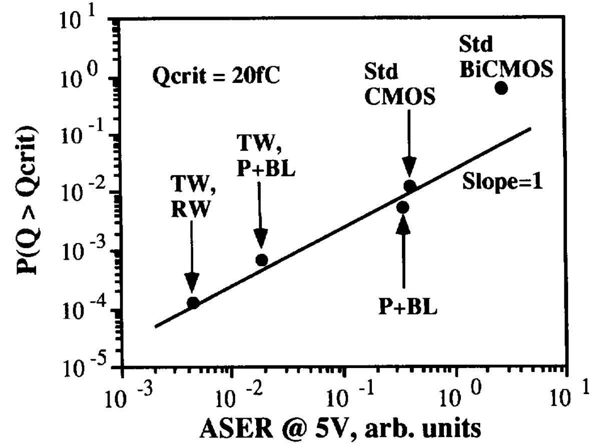

Figure 3. Correlation of charge-collection and ASER data. Excellent agreement is shown between projected ASER @ 5V and the charge-collection data with Qcrit=20fC.

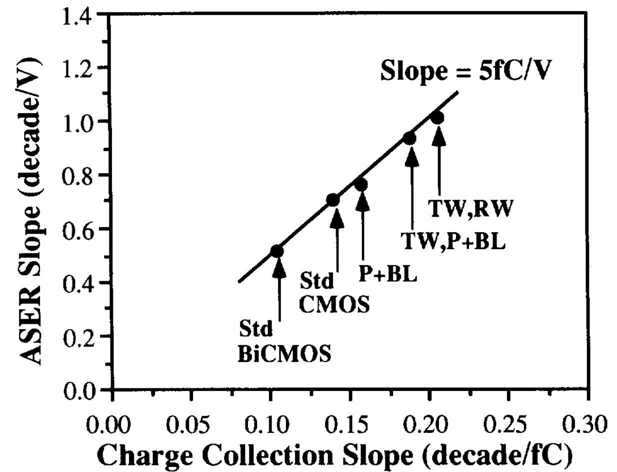

Figure 4. The slope of the ASER data in Figure 2 is proportional to the charge collection slope in Figure 1 for the different distributions. The multiplying factor is 5 fC/V as predicted by Equation (2).

Process Descriptions

A schematic cross-section of the 0.5 µm BiCMOS process is shown in Figure 5(a). For this process, the simplest method of forming an n-well under the array p-well is to extend the n+ buried

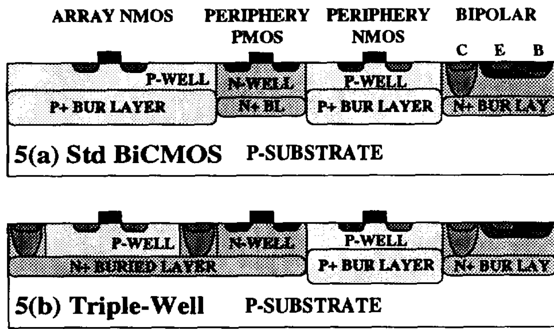

Figure 5(a). Schematic cross-section of the standard BiCMOS architecture. (b). Schematic cross-section of the triple-well BiCMOS architecture.

layer (Figure 5(b)) [14]. Simulated p-well doping profiles for the standard BiCMOS and elevated p+ buried layer processes are shown in Figure 6(a). The peak doping for the elevated p+ buried layer, referred to as "P+BL", is approximately 3E18/cm^3, creating a more effective barrier to alpha strikes. The P+BL dose, however, must not be allowed to increase the NMOS Vt or bipolar collector-substrate capacitance too much.

For the triple-well process, additional doping is needed in the p-well to provide adequate isolation between the n+ source/drain and n+ buried layer and to decrease the pinched p-well sheet resistance to allow proper NMOS operation. The first method for increasing the p-well doping in the triple-well, referred to as "TW,PBL", includes the p+ buried layer doping under the array. Because boron diffuses faster than arsenic, the p+ buried layer doping increases the doping at the bottom of the p-well, as seen in Figure 6(b). The second method for increasing the p-well doping in the triple-well, referred to as "TW,RW", uses a high energy boron implant to form a retrograde p-well, as seen in Figure 6(b). The p+ buried layer dose for the TW,PBL process is limited by the increase in NMOS Vt and bipolar Ccs parameters, while the TW,RW implant is limited by the increase in NMOS Vt. The triple-well data and profiles represent the largest allowable doses.

Device Characteristics

Reverse I-V measurements of the n+ source/drain (S/D) to p-well junction were made for the triple-well devices with the n+ buried layer and p-well grounded. Figure 7 shows the n+ S/D voltage at 1 µA as a function of dose for the two triple-well processes. N+ S/D to N+ BL punchthrough occurs for the lower doses, while higher doses decrease the breakdown voltage due to the higher doping. The punchthrough problem is also exhibited in isolation leakage measurements between adjacent n+ S/D regions as shown in Figure 8. The normalized dose of 5 is necessary to provide adequate isolation for the TW,P+BL process, while a normalized dose of 0.5 or greater is necessary in the TW,RW process. Because the n+ buried layer pinches off the bottom of the

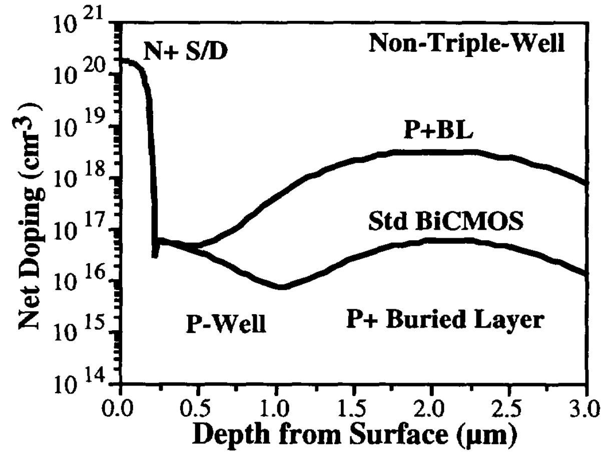

Figure 6(a). P-well doping profiles for the standard BiCMOS process and for the elevated p+ buried layer (P+BL) process.

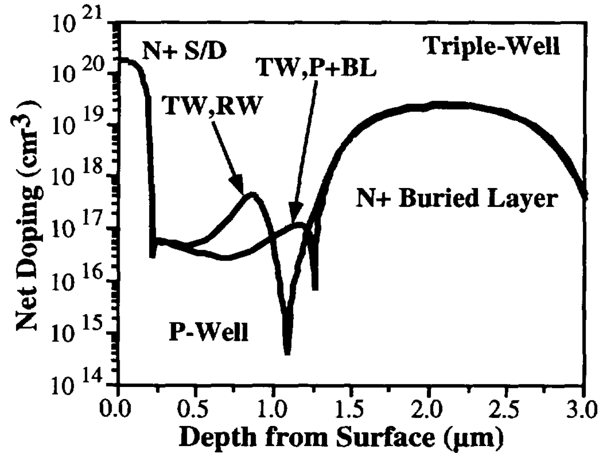

Figure 6(b). P-well profiles for the two triple-well approaches. TW,P+BL uses an elevated p+ buried layer dose to increase the doping at the bottom of the well, while TW,RW uses a retrograde well.

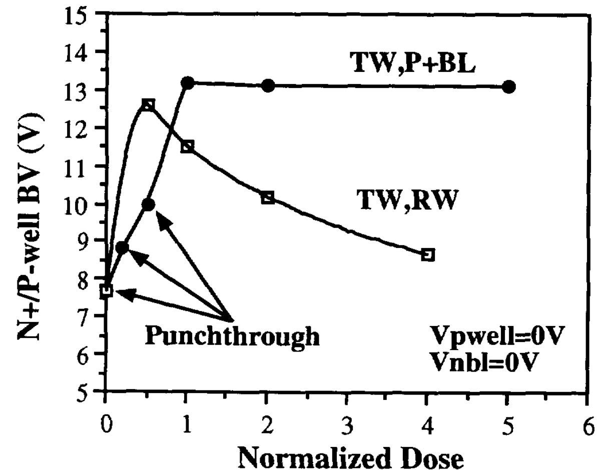

Figure 7. Punchthrough and breakdown voltage of n+ S/D to p-well with the buried layer grounded for the triple-well structures.

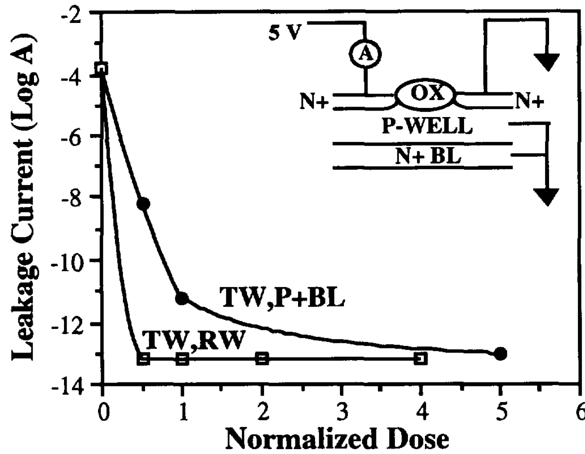

Figure 8. Leakage current between active areas across field oxide for the triple-well structures.

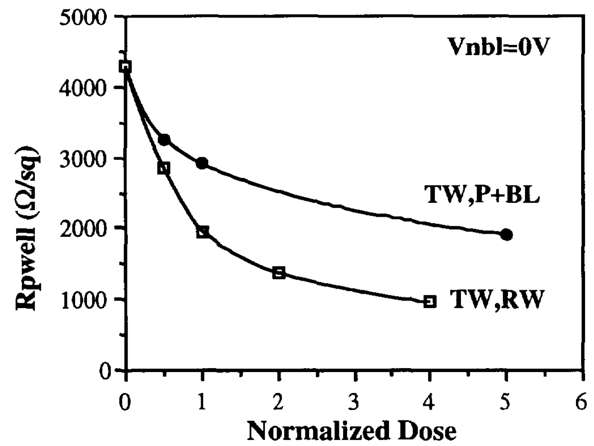

Figure 9. Pinched p-well sheet resistance for the triple-well structures.

p-well (Figure 6(b)), the p-well sheet resistance can be increased substantially, which can cause the forward bias of the source/p-well junction if Isub*Rwell > 0.6 V. The p-well sheet resistance decreases with increasing dose (Figure 9), with a normalized dose of 5 for the TW,P+BL and 1 for the TW,RW processes providing acceptable values. The forward-biasing of the source/p-well junction is quantified in Figure 10 by measuring the drain voltage at Vg=5V required to give Id=2*Id(Vg=Vd=5V). A larger Vd is required to turn on the source/substrate junction with increasing dose.

The impact of the triple-well process on Vt is shown in Figures 11 and 12. Vt increases only slightly for the TW,P+BL process over this range of doses, while the P+BL process exhibits a much stronger increase. The normalized dose of 5 in these two processes represents the largest allowable dose without a detrimental increase in Ccs. For the TW,RW process the 130 mV increase in Vt at a normalized dose of 2 is too large, but the 40 mV increase at 1 is acceptable. Correspondingly, the Vt change with back-bias (Figure 12) follows the trend in Figure 11 with the P+BL process showing the largest body factor, followed next by the TW,RW process and finally by the TW,P+BL process. These results are in good agreement with the simulated profiles in Figure 6.

Conclusions

In conclusion, dramatic improvements in SER can be achieved without compromising device performance. A 8X reduction in BiCMOS SER is realized with an elevated p+ buried layer, while a 600X reduction is achieved with a triple-well process. Diode charge collection and ASER measurements show excellent agreement for the calculation of failure rate and the V_{CC} dependence of failure rate.

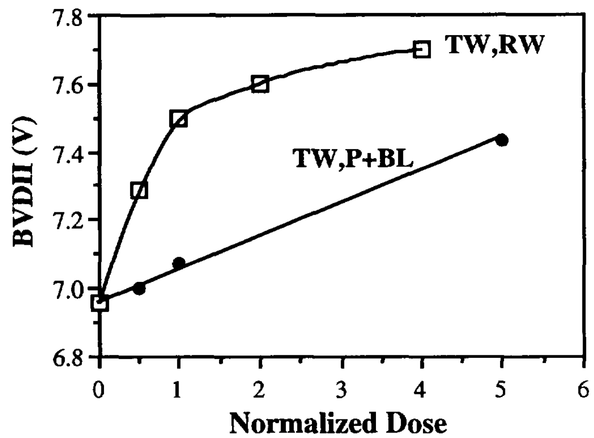

Figure 10. Drain voltage necessary for Id=2*Id(Vd=5V) at Vg=5V for the triple-well processes.

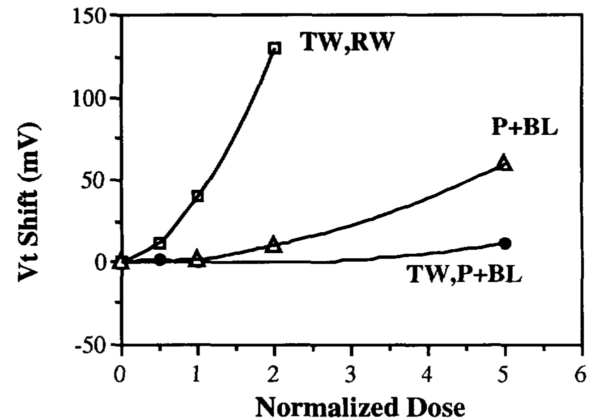

Figure 11. Vt increase with dose for the elevated buried layer and triple-well processes (Lg=0.6μm).

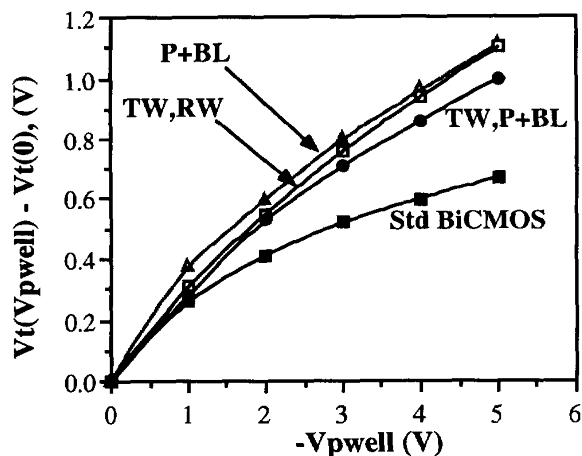

Figure 12. Vt increase with p-well back-bias for the BiCMOS processes (Lg=0.6μm).

Acknowledgments

The authors would like to thank Bob Dunnigan and Mike Kraft for their help with the packaging and measurements, Kelly Baker, Larry Childs, and Howard Kirsch for their useful discussions, and Rick Sivan and Lou Parrillo for their support and guidance throughout this project.

References

[1] T. May and M. Woods, "Alpha-particle-induced soft errors in dynamic memories," IEEE Trans. on Elect. Dev., **ED-26**, pp. 2, 1979.

[2] D. Yaney, J. Nelson, and L. Vanskike, "Alpha-particle tracks in silicon and their effect on dynamic MOS RAM reliability," IEEE Trans. on Elect. Dev., **ED-26**, pp. 10, 1979.

[3] G. Sai-Halasz, M. Wordeman, and R. Dennard, "Alpha-particle-induced soft error rate in VLSI circuits," IEEE Trans. on Elect. Dev., **ED-29**, pp. 725, 1982.

[4] H. Momose, T. Wada, I. Kamohara, M. Isobe, J. Matsunaga, and H. Nozawa, "A p-type buried layer for protection against soft errors in high density CMOS static RAMs," IEDM Tech. Dig., pp. 706, 1984.

[5] S. Fu, A. Mohsen, and T. May, "Alpha-particle-induced charge collection measurements and the effectiveness of a novel p-well protection barrier on VLSI memories," IEEE Trans. on Elect. Dev., **ED-32**, pp. 49, 1985.

[6] B. Chappell, S. Schuster, and G. Sai-Halasz, "Stability and SER analysis of static RAM cells," IEEE Trans. on Elect. Dev., **ED-32**, pp. 463, 1985.

[7] S. Voldman, P. Corson, L. Patrick, K. Nguyen, L. Gilbert, R. Goodwin, T. Maffit, and S. Murphy, "CMOS SRAM alpha particle modelling and experimental results," IEDM Tech. Dig., pp. 518, 1987.

[8] P. Carter and B. Wilkins, "Influences on soft error rates in static RAM's," IEEE J. of Solid-State Circuits, **SC-22**, pp. 430, 1987.

[9] S. Murakami, K. Ichinose, K. Anami, and S. Kayano, "Improvement of soft-error rate in MOS SRAM's," IEEE J. of Solid-State Circuits, **SC-24**, pp. 869, 1989.

[10] T. Mele, J. Hayden, F. Walczyk, M. Lien, Y. See, D. Denning, S. Cosentino, and A. Perera, "A high performance 0.5μm BiCMOS triple polysilicon technology for 4Mb fast SRAMs," IEDM Tech. Dig., pp. 481, 1990.

[11] T. Toyabe, T. Shinoda, M. Aoki, H. Kawamoto, K. Mitsusada, T. Masuhara, and S. Asai, "A soft error rate model for MOS dynamic RAM's," IEEE J. of Solid-State Circuits, **SC-17**, pp. 362, 1982.

[12] W. Krautschneider and W. Meyberg, "Prediction of soft error rate of 4 Mbit DRAM," ESSDERC Tech. Dig., pp. 709, 1987.

[13] S. Kirkpatrick, "Modeling diffusion and collection of charge from ionizing radiation in silicon devices," IEEE Trans. on Elect. Dev., **ED-26**, pp. 1742, 1979.

[14] Y. Okazaki, T. Kobayashi, S. Konaka, T. Morimoto, M. Takahashi, K. Imai, and Y. Kado, "New well structure for deep sub-μm CMOS/BiCMOS using thin epitaxy over buried layer and trench isolation," VLSI Tech. Dig., pp. 83, 1990.