AN ADVANCED 0.8 μm COMPLEMENTARY BICMOS TECHNOLOGY FOR ULTRA-HIGH SPEED CIRCUIT PERFORMANCE

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ABSTRACT

A 0.8 μm fully Complementary BiCMOS (CBiCMOS) process has been developed which offers superior drive capability and low voltage performance compared to standard BiCMOS technologies. The CBiCMOS process was developed by the successful integration of a high performance, poly emitter vertical PNP (F_t=6.5 GHz) into a core BiCMOS technology containing high performance NPN bipolar (F_t=17 GHz, ECL gate delay = 65 ps) and CMOS transistors (CMOS gate delay = 68 ps). A CBiCMOS push-pull ring oscillator has been fabricated with a gate delay of 250 ps for a 1 pF load; this is believed to be the fastest loaded ring gate delay ever reported for gate lengths down to 0.6 μm. This new CBiCMOS technology is expected to play an important role in the development of future generations of high speed memories (i.e. 4-Mbit ECL I/O SRAM's and beyond) which will require novel process technologies to avoid the deleterious effects of reduced voltage operation.

INTRODUCTION

The next-generation of high-speed 4-Megabit ECL I/O SRAM's must operate at reduced power supply voltages to minimize reliability concerns. It has been recently reported that operation at reduced voltages will require novel process technologies to maintain circuit performance, with CBiCMOS being the technology offering the best low voltage operation [1,2]. In addition, several high-performance CBiCMOS processes were recently reported; bipolar F_t's of 8-12 GHz (NPN) and 2.5-5 GHz (PNP), and loaded ring delays of 250ps at 0.3 pF loading were obtained [3,4,5]. Using an advanced 0.8 μm BiCMOS technology [6] for high-performance 1-Megabit ECL I/O SRAM's (average access time less than 7ns [7]) as the core technology, we report the successful development of a high-performance, fully Complementary BiCMOS (CBiCMOS) technology which offers not only superior performance compared to BiCMOS at reduced power supply voltages, but at 5V supplies as well.

PROCESS TECHNOLOGY

The core 0.8 μm BiCMOS technology features an advanced, fully-recessed oxide isolation, 150 Å gate oxide, a silicided polysilicon local interconnect scheme, two levels of polysilicon, and two levels of metal (see Tables 1 and 2 for process sequence and key technology features, respectively, and reference [6] for additional core process details). The NMOS and PMOS transistors incorporate LDD implants, while the NPN and PNP transistors have self-aligned poly-emitter architectures. Poly-1 is used for the MOS gate, while poly-2 forms ECL load resistors and a silicided local interconnect layer, in addition to the poly-emitters.

The development of this advanced CBiCMOS process has focused on the fabrication of a high performance poly-emitter vertical PNP transistor (see Fig. 1 for an illustration of the device cross-section). The PNP transistor utilizes a phosphorus implanted base and a boron doped polysilicon emitter. The collector region, including heavily doped sub-collector, are formed in the P-Well over P-Buried layer used by the NMOS circuit elements. The nominal emitter length for both bipolar transistors is 0.8 μm.

BIPOLAR CHARACTERISTICS

The CBiCMOS performance is heavily driven by the bipolar transistor characteristics; this paper will thus focus on the PNP and NPN characteristics. Fig's 2 and 3 present the Gummel plots, Beta vs. Ic, and Ic-Vce characteristics for the PNP and NPN transistors, respectively. The low Iceo leakage and negligible E-B depletion layer recombination current indicate very high quality poly emitter bipolar transistors. The peak Beta's are 100 and 130 for the PNP and NPN, respectively. Especially note the flat Beta vs Ic characteristics of the PNP transistor (flat over five orders of magnitude Ic), indicating excellent E-B junction characteristics.

F_t vs. collector current density (Jc) measurements of 0.8 μm PNP and NPN transistors are shown in Fig. 4; the peak F_t's are 6.5 GHz and 17 GHz for the PNP and NPN, respectively; the bipolar transistor performance is state-of-the-art for even a pure bipolar process. Fig. 5 shows plots of the dependence of F_t on the collector sink resistance Rc for both transistor types (curves obtained by varying the epi thickness and well drive). Since the CBiCMOS process does not employ a high energy sink implant to reduce this parasitic resistance, further performance improvements are possible, if required, for specific applications.

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RING OSCILLATOR PERFORMANCE

There are a number of layout options for the CBiCMOS ring oscillator. For the data to be presented here, a CBiCMOS ring oscillator using a push-pull output driver is employed (see Fig. 6 for a circuit schematic). A merged layout was chosen in which the extrinsic base of the NPN is formed in the P+ S/D diffusion of the PMOS transistor, reducing the parasitic resistances and capacitances while improving the packing density; the PNP and the N+ S/D are similarly designed. Fig.7 presents the dependence of the CBiCMOS push-pull ring oscillator gate delay with 1 pF load and 5 Volt supply on the bipolar sink resistance. The 250 ps gate delay is believed to be the fastest ever reported for a 1 pF load, even for processes with drawn gate dimensions down to 0.6 μm. For comparison, a similar BiCMOS ring has a gate delay of about 340 ps, while the equivalent pure CMOS ring has a gate delay of over 500 ps. Clearly, there are significant performance advantages to the CBiCMOS-based designs using today's leading edge 5 V compatible processes.

Fig. 8 demonstrates the superior performance of the CBiCMOS gate delay compared to a BiCMOS gate as the supply voltage is reduced to next generation levels (~3.3 V). Utilizing the unique design capabilities provided by the CBiCMOS process will facilitate enhancing the performance of next generation 4 Megabit ECL SRAM's, even as the supply voltage is reduced. Other designs could also leverage the added flexibility of CBiCMOS designs into higher performance parts, all for a negligible increase in fabrication complexity.

Table I: Process Sequence Outline

* Twin Buried Layer	* N^+, P^+ Poly-2 Implants
* 1.1 μm Intrinsic Epi	* Emitter Drive
* Twin Well	* $TiSi_2$ Formation
* Recessed Oxide Isolation	* Contact Dielectric
* Gate + Poly-1	* Contact Formation
* LDD Formation	* Tungsten Plugs
* N^+ S/D Implant	* Metal-1
* Base Implants	* Intermetal Dielectric
* P^+ S/D Implant	* Via Formation
* Interpoly Oxide	* Tungsten Plugs
* Poly-2 Deposition	* Metal-2
* Load Resistor Implant	* Passivation

SUMMARY

A 0.8 μm fully Complementary BiCMOS (CBiCMOS) process has been developed which offers superior drive capability and low voltage performance compared to standard BiCMOS technologies. The CBiCMOS process was developed by the successful integration of a high performance, poly emitter vertical PNP (F_t=6.5 GHz) into a core BiCMOS technology containing high performance NPN bipolar (F_t=17 GHz, ECL gate delay = 65 ps) and CMOS transistors (CMOS gate delay = 68 ps). A CBiCMOS push-pull ring oscillator has been fabricated with a gate delay of 250 ps for a 1 pF load; this is believed to be the fastest loaded ring gate delay ever reported for gate lengths down to 0.6 μm.

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[7] B. Kertis *et al.*,to be published, 1990 Symposium on VLSI Circuits.

Table II: Key Technology Features

* 17 Masks	* 1.5 μm Poly Pitch
* 1.1 μm Intrinsic Epi	* "Contactless" Technology
* Recessed Oxide Isolation	* Local Interconnect
* 1.5 μm Isolation Pitch	* Tungsten Plugs
* 150Å Gate Oxide	* 1.8 μm Metal Pitch
* Double Polysilicon	* Double Metal
* MOS L_{drawn} = 0.8 μm	* Full Planarization

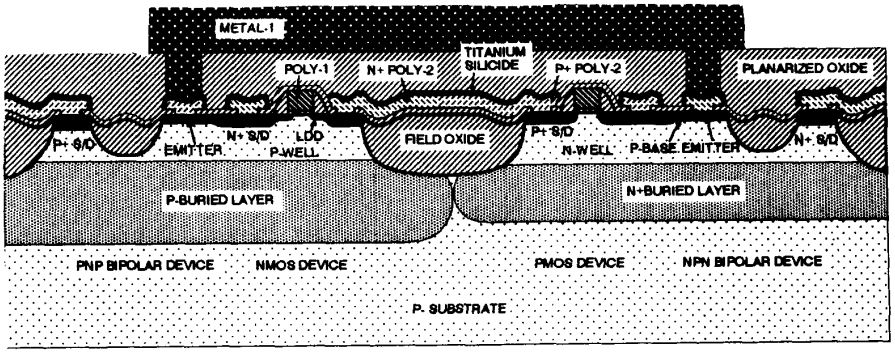

Fig. 1: Schematic cross-section of the CBiCMOS process architecture through Metal-1.

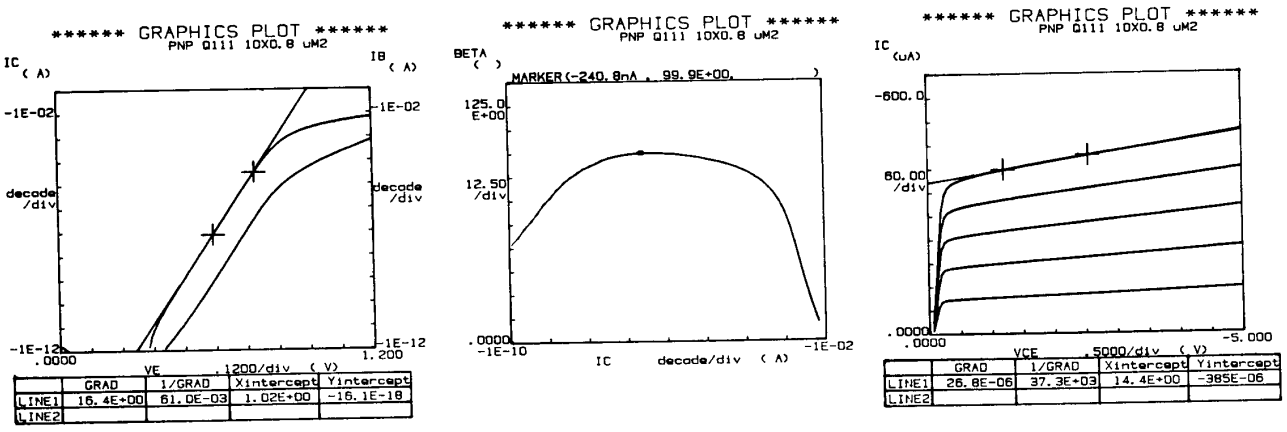

Fig. 2: Gummel plots, Beta vs Ic, and Ic-Vce for PNP bipolar transistors.

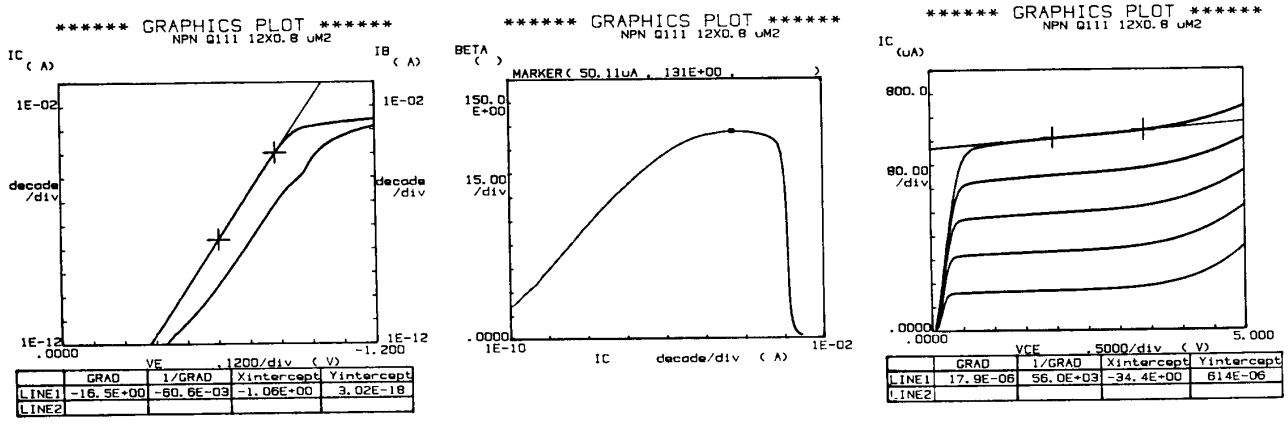

Fig. 3: Gummel plots, Beta vs Ic, and Ic-Vce for NPN bipolar transistors

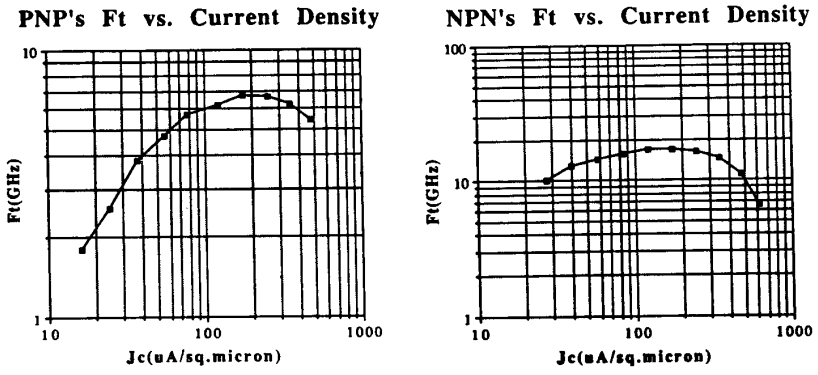

Fig. 4: Ft vs collector current density Jc for the PNP and NPN transistors.

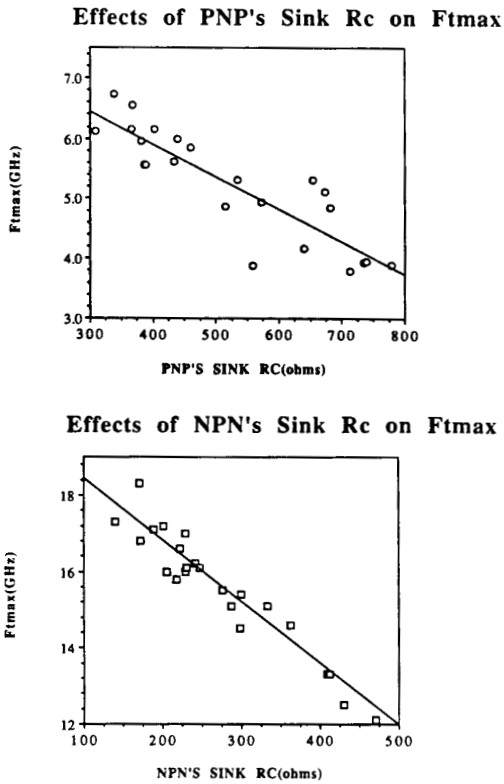

Fig. 5: Plots of Ft vs the collector sink resistance Rc for the PNP and NPN transistors.

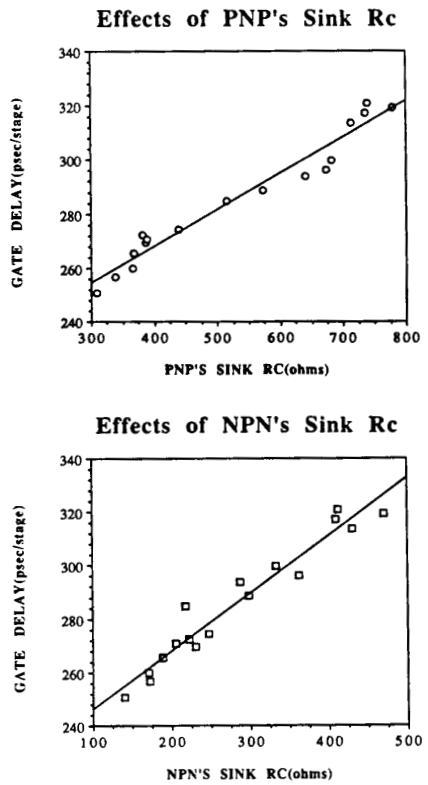

Fig. 7: CBiCMOS push-pull ring oscillator performace for variations in the collector sink resistance for a load of 1 pF. Device dimensions are: Wn=10μm, Wp=15μm, We=5μm, and Wepnp=10μm.

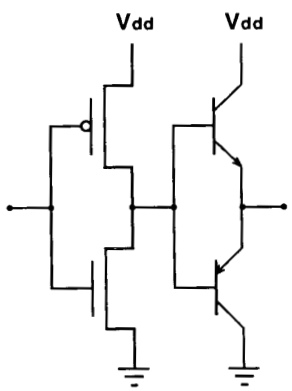

Fig. 6: Circuit schematic of the CBiCMOS push-pull ring oscillator.

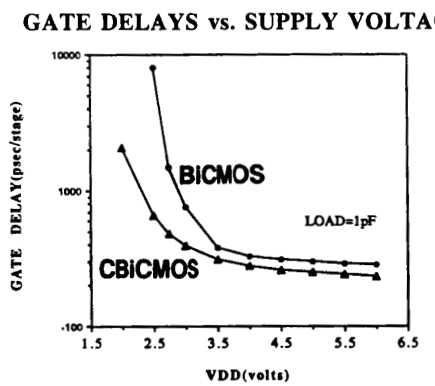

Fig. 8: Gate delay of CBiCMOS and BiCMOS ring oscillators vs supply voltage.