AN ADVANCED SELF-ALIGNED BICMOS TECHNOLOGY FOR HIGH PERFORMANCE 1-MEGABIT ECL I/O SRAM'S

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ABSTRACT

An advanced self aligned BiCMOS technology has been developed for high-performance 1-Megabit ECL I/O SRAM's. The 0.8 μM technology features include an advanced, fully-recessed oxide isolation, a silicided polysilicon local interconnect scheme, two levels of polysilicon, and two levels of metal with tungsten plugs. These process features combine to produce MOS gate delays in the 100ps range, and bipolar transistors with F_T's of 15 GHz. The manufacturability of the technology has been demonstrated by the successful fabrication of a scaled 256K ECL I/O SRAM.

INTRODUCTION

BiCMOS is widely recognized as a superior processing technology capable of integrating the high packing density of pure CMOS with the high performance of bipolar into a single process technology [1-4]. A 1.0 μM BiCMOS technology (BiCMOS-III), currently used for the production of 256K ECL I/O SRAM's, has been previously described [1]; the next generation 0.8 μM BiCMOS technology (BiCMOS-IV), optimized for a high performance 1-Meg ECL I/O SRAM, is presented in this paper. Included are a detailed description of the process technology, MOS and bipolar transistor performance, and ring oscillator circuit performance.

PROCESS TECHNOLOGY

The 0.8 μM BiCMOS technology is an optimized, self-aligned, fully planarized, double poly, "contactless" double metal process. Fig. 1 illustrates a cross-section through the devices. Table I presents an outline of the process sequence, while Table II itemizes the key technology features. Taguchi experimental design techniques have been extensively used to develop an optimized, manufacturable process. Self-aligned twin buried layers are defined for the NMOS, PMOS, and bipolar transistors. The buried layers provide a high degree of latch-up immunity, reduced isolation spacing, and soft error immunity. A one micron intrinsic epitaxial layer is deposited by reduced pressure epitaxy, followed by the formation of self-aligned N- and P-well regions. Together with the N^+ and P^+ buried layers, the final well doping profiles are retrograde, facilitating the fabrication of high performance, sub-micron devices. Active regions are defined by an optimized, fully planarized, recessed oxide isolation process. Total encroachment is less than 0.1 μM for 7500Å field oxide. Cross-section SEM indicates that the recessed oxide isolation forms oxide isolated S/D and base junctions, significantly reducing device parasitic capacitances and improving performance.

The MOS transistors are formed by a masked LDD implant, sidewall spacer formation, N^+ and P^+ S/D implants, and RTA junction annealing. The gate electrode for the NMOS and PMOS transistors is N^+ doped polysilicon. The bipolar transistors are self-aligned, submicron silicided poly structures formed by poly-2. Fig. 2 shows a SIMS profile of the As and B profiles in the emitter of the bipolar transistor.

The poly-2 layer is also used to form high resistance poly load resistors for the SRAM memory cell. N^+ and P^+ poly-2 with and without self-aligned $TiSi_2$ (the silicided N^+ and P^+ poly-2 sheet resistances are less than 2 ohm/square) provide the circuit designer with a broad range of sheet resistance values and low- resistance local interconnects. In addition, all "contacts" to single crystal silicon are made through silicided N^+ and P^+ doped poly-2; this technology permits the contact to overlap the field region, resulting in a high density layout with reduced parasitic capacitance. Tungsten plug technology (see Fig. 3)

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and a sandwiched Al/Si/Cu metallurgy are used at both metal levels to provide a reliable, low-resistance interconnect system.

DEVICE CHARACTERISTICS

NMOS and PMOS Transistors

Fig. 4 illustrates the subthreshold I-V characteristics of 0.6 μM Leff NMOS and PMOS transistors; the subthreshold slopes for both the PMOS and NMOS transistors are 92 mV/decade. Fig. 5 shows the dependence of punchthrough voltage on Leff, demonstrating the high resistance to punchthrough provided by the well profiles for gate lengths down to 0.5 μM.

Bipolar Transistor

Fig. 6 presents the Gummel and Beta vs. Ic characteristics of a typical 0.8 μM emitter length bipolar transistor. The relatively flat Beta characteristics, in addition to the low Iceo leakage, are indicative of high quality poly emitter bipolar transistors. F_T vs. collector current density (Jc measurements of a 0.8 μM transistor are shown in Fig. 7, with a peak F_T of 14.6 GHz. The bipolar transistor performance in BiCMOS-IV is comparable or superior to many pure bipolar processes.

Ring Oscillator

Fig. 8 compares the gate delays for CMOS, ECL, and BiCMOS ring oscillators under various loading conditions. Fig. 9 compares ring gate delays for BiCMOS-III vs. BiCMOS-IV, demonstrating the significant performance advantages offered by BiCMOS-IV.

LINEAR SHRINK 256K ECL I/O SRAM

The 256K ECL I/O SRAM was processed through a linear shrink and successfully fabricated using the BiCMOS-IV process technology (see Fig. 10 for a die photograph); fully functional die were obtained.

SUMMARY

An advanced 0.8 μM BiCMOS technology for a high performance 1 Meg ECL I/O SRAM is described. Advanced features include fully recessed oxide isolation, two levels of polysilicon, two levels of metal with tungsten plugs, and a silicided poly-Si local interconnect scheme to improve manufacturability and enhance performance. These features combine to produce MOS gate delays in the 100ps range, and bipolar transistors with F_T's of 15GHz. The manufacturability of the technology has been demonstrated by the successful fabrication of a scaled 256K SRAM.

ACKNOWLEDGMENTS

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Table I: Process Sequence Outline

* Twin Buried Layer
* 1.1 μM Intrinsic Epi
* Twin Well
* Recessed Oxide Isolation
* Gate + Poly-1
* LDD Formation
* N^+ S/D Implant
* Base Implant
* P^+ S/D Implant
* Interpoly Oxide
* Poly-2 Deposition
* Load Resistor Implant
* Poly-2 Implants
* TiSi2 Formation
* Contact Dielectric
* Contact Formation
* Tungsten Plugs
* Metal-1
* Intermetal Dielectric
* Via Formation
* Tungsten Plugs
* Metal-2
* Passivation

Table II: Key Technology Features

* 17 Masks
* 1.1 μM Intrinsic Epi
* Recessed Oxide Isolation
* 1.5 μM Isolation Pitch
* 150Å Gate Oxide
* Double Polysilicon
* MOS L_{drawn} = 0.8 μM
* 1.5 μM Poly Pitch
* "Contactless" Technology
* Local Interconnect
* Tungsten Plugs
* 1.8 μM Metal Pitch
* Double Metal
* Full Planarization

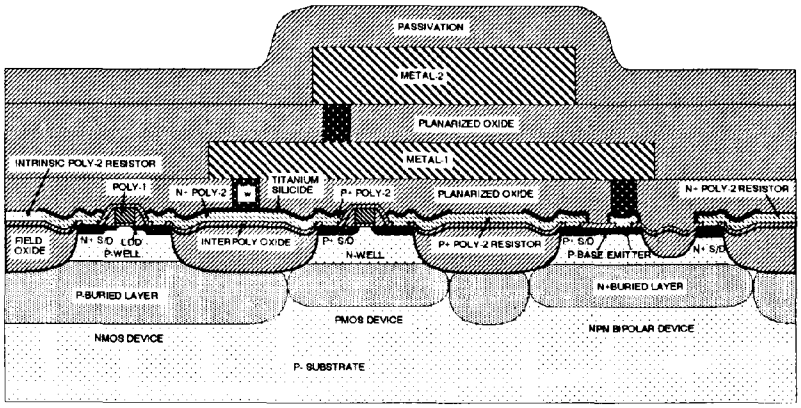
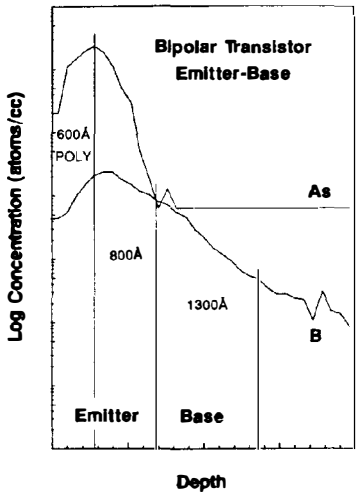


Fig. 1: Schematic cross-section of the BiCMOS-IV process architecture.

Fig. 2: SIMS profiles of the As and B impurity concentration profiles through the emitter-base region. The emitter-base junction depth is 800Å, while the metallurgical base width is 1300Å.



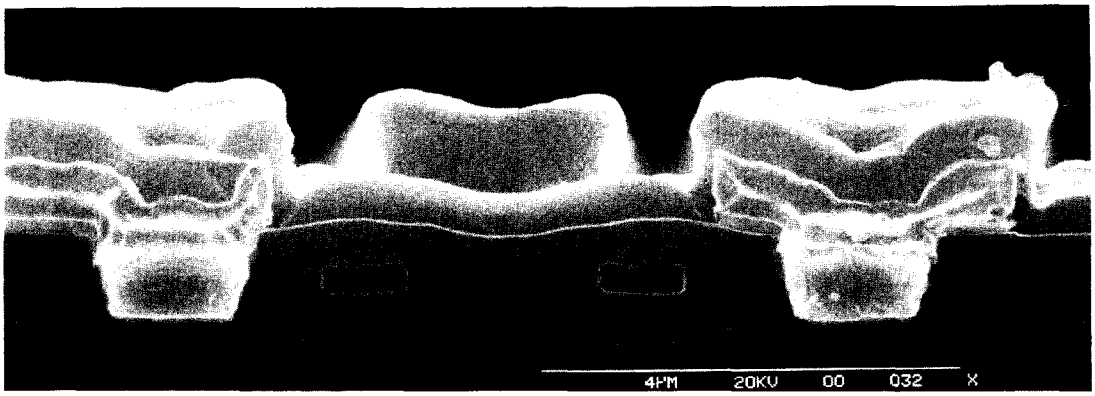


Fig. 3: SEM cross-section of Tungsten plug with Metal-1.

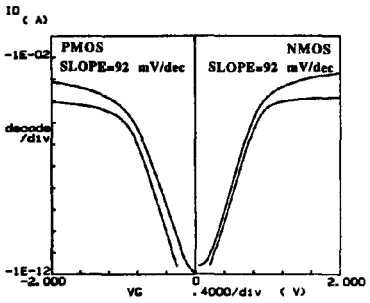


Fig. 4: Subthreshold I-V characteristics of 0.6 μM Leff MOS transistors for $|V_{ds}|$ = 0.10V and 5.0V.

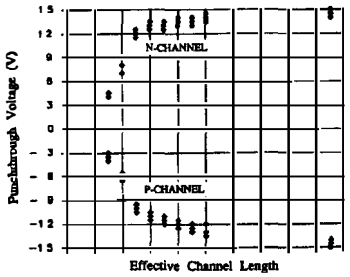
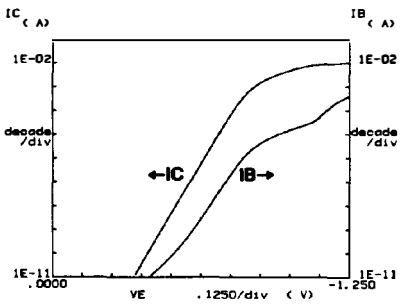


Fig. 5: MOS punchthrough voltage vs. Leff.



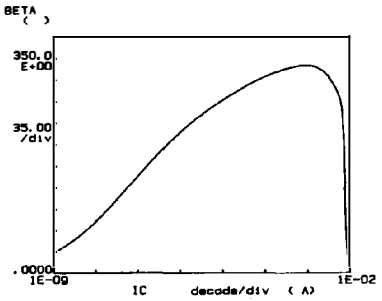


Fig. 6: Bipolar transistor Gummel and Beta vs. I_C plots for 0.8 μM emitter length

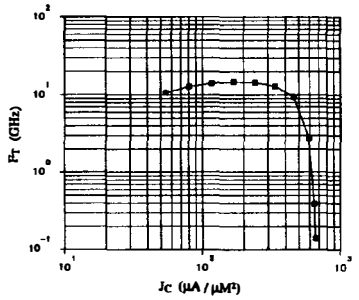


Fig. 7: F_T vs. collector current density J_C. The peak value of F_T is 14.6 GHz.

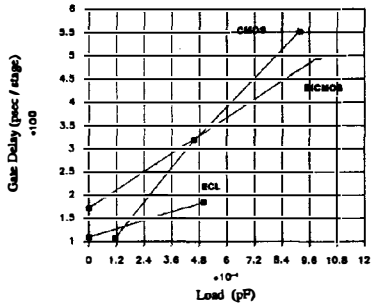


Fig. 8: Gate delay vs. loading for CMOS, ECL, and BiCMOS ring oscillator circuits.

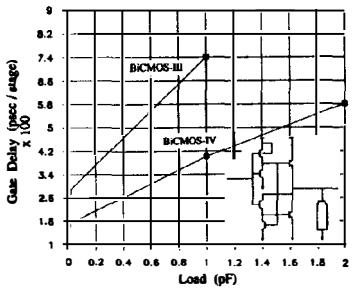


Fig. 9: Comparison of the gate delay for BiCMOS-III and BiCMOS-IV technologies.

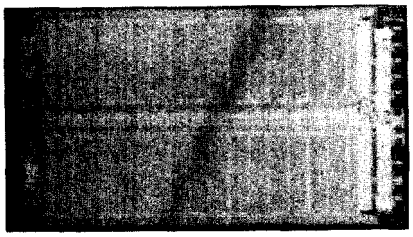


Fig. 10: Die photo of BiCMOS-IV fabricated 256K ECL I/O SRAM after a linear shrink.