17.2 A Highly Versatile 0.18um CMOS Technology With Dense Embedded SRAM

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ABSTRACT

We report on a 3.3V/2.5V compatible, 1.5V high performance dense CMOS SRAM technology utilizing a 2.74 um^2 6-T Bitcell. This 0.18μm CMOS process with a nominal 0.13μm gate poly and a 30Å gate oxide utilizes aggressive inter-well isolation, enhanced self-aligned local interconnect, low-K interlevel dielectric, and scaled copper metalization. In addition, the technology allows for low leakage, high density and SER resistant Embedded SRAM applications by allowing integration of low leakage array transistors, Buried Channel pMOS loads, self-aligned contacts and Triple Well in the memory array. Finally, this integration includes a 70Å/30Å DGO technology for 3.3V interfaces. High performance 6-T bitcell operation, 8Mb stand-alone SRAM yield and high performance DSP circuit with 4Mb embedded memory with this aggressively scaled bitcell has been successfully demonstrated. Cell currents of 85μA has been achieved for a supply voltage of 1.5V while maintaining static noise margin in excess of 220mV

INTRODUCTION

High performance workstation and server systems require ultra-fast SRAM chips with high density, low power, fast clock rate and low cost. The logic based SRAM technology described in this work is suitable for stand-alone as well as embedded system applications. The 6-T transistor CMOS SRAM technology utilizes 0.13±0.02 μm gate length, 30Å gate oxide periphery and array transistors based on shallow trench isolation, retrograde well, Co salicide, and dual in-laid copper metalization from the technology platform [1]. To realize the unique requirements of scaled cell area, stable and high speed cell operation for SRAM array [2-3], process enhancement such as aggressive active spacing of 0.21μm and n+ to p+ isolation down to 0.42μm, capped gate array transistors with low leakage current, 0.18μm self-aligned local interconnect, and low K interlevel dielectric film has been developed. In order to realize the three different flavors of transistors namely, (i) 30Å high performance, (ii) 30Å low leakage with triple well and (iii) 70Å 3.3V I/O, significant integration and implant optimization was involved. Table 1 shows the salient technology features and in the following sections, we discuss the process integration steps required to achieve these electrical characteristics.

PROCESS INTEGRATION

The SRAM process is based on a high performance core CMOS platform technology in which SRAM serves as an enhanced add-on module. Figs. 1-2 show SRAM cell array cross-section and the cell layout, respectively. For scaled SRAM cell area requirement, active spacing of 0.21μm and n+ to p+ spacing down to 0.42 μm with a triple well option have been achieved with optimized photo and implant conditions (Fig. 3). Surface channel nMOS and buried channel pMOS transistors with dielectric capped gate and low leakage current characteristics are used to enable the formation of self-aligned local interconnect in which gate poly features are electrically isolated from the local interconnect. Extensive optical proximity correction (OPC) has been utilized in the mask layout (as shown in Fig. 2) for critical levels and an anti-reflect film is used in the dielectric stack to optimize the photo printing characteristics for gate and local interconnect layers. The self-aligned local interconnect is defined by selectively etching the in-laid features as small as 0.18μm with respect to an etch stop layer. DGO transistors with 70Å gate oxide are also integrated for 3.3/2.5V I/O operations. For enhanced SRAM speed operation, a low-K interlevel dielectric film with a dielectric constant of 3.5 (vs. 4.1 for conventional TEOS ILD layers) is used. The process is completed using a 5-level scaled in-laid Cu metalization.

ELECTRICAL RESULTS

As is clear from the versatility of this integration, 3 different sets on N- and P-FETs have to be optimized. Fig. 4 shows the sequence of process steps required to achieve the different transistor targets without compromising the performance of any. Since the scaling of BCPFET is the most challenging, careful optimization of the BCPFET channel is done by increasing both boron and retrograde well (antimony) doses. A narrow width and high concentration counterdoped layer which is unaffected by the DGO heat is realized and excellent Vt roll-off is achieved (Fig. 5). As seen from Fig. 4 only two additional reticles are used for the DGO integration in order to keep the process cost effective. This implies the channel implants cannot be optimized separately for both transistors, therefore making simultaneous Vt targeting for 30A core and 70A I/O transistors a difficult task. Channel dopant segregation during DGO heat poses an additional challenge. A low doped channel in conjunction with heavy halo approach is used to get around the problem of Vt lowering during DGO process as shown in Fig. 6. Fig. 7 shows leakage current distribution from self-aligned local interconnect and self-aligned contact array test structures. While maintaining low leakage SALI and SAC characteristics for the SRAM array, a low metal-LI-active contact resistance is achieved (Fig. 8) which is critical for a low bitline parasitic. The low-K ILD layer used in the process can further reduce parasitic capacitance by 14% as compared with conventional TEOS ILD, thus improving circuit speed performance. Fig. 9 shows in-laid Cu interconnect sheet resistance for metal 1 to metal 5. The minimum metal length is scaled to 0.28μm and the minimum contact/via sizes are 0.25μm/0.315 μm, respectively for this technology generation. Fig. 10 shows the SRAM cell transfer characteristics and cell current. A cell current of 85μA has been achieved for a supply voltage of 1.5V while maintaining the static noise margin in excess of 220mV. The SRAM array transistors use a cell ratio of 1.25 with drive W/L of 0.23μm/0.13μm. As mentioned before, the overall bitcell leakage is ~1pA at room teperature. This is achieved with low leakage BCPFET loads and low leakage latch gates. Fig. 11 shows bitcell leakage and the various components of leakage in the bitcell over temperature.

CONCLUSIONS

A high performance 1.5V CMOS Embedded SRAM technology has been developed and demonstrated on a 2.74μm^2 cell area using aggressive interwell isolation, self-aligned local interconnect, low-K ILD layer, and scaled in-laid Cu metallization. A cell current of 85μA and a static noise margin of 220mV at 1.5V have been achieved.

ACKNOWLEDGMENTS

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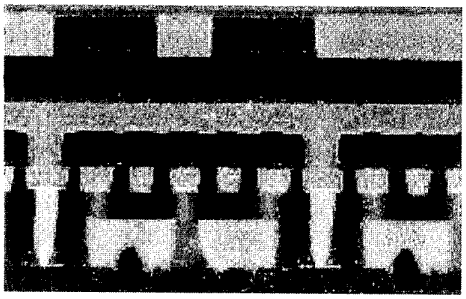

Fig.1 SEM cross-section of SRAM cell array using self-aligned local interconnect and scaled in-laid Cu metallization.

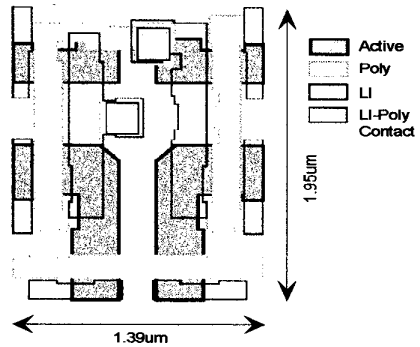

Fig.2 SRAM cell layout with a cell area of 2.74μm^2.

Tab. 1 Technology Parameters

Supply Voltage (V)	1.5
Gate Oxide (nm)	3
Gate Length (um)	0.13
Active Pitch (um)	0.42
n+ - p+ Space (um)	0.42
Local Interconnect Width (um)	0.18
Metal Pitch (um)	0.66
Contact Size (um)	0.25
Via1 Size (um)	0.37
Core nMOS Vt (V)	0.32
Core nMOS Ids/W (uA/um)	650
Core nMOS Leakage (nA/um)	0.2
Core pMOS Vt (V)	-0.32
Core pMOS Ids/W (uA/um)	-275
Core pMOS Leakage (nA/um)	0.2
Array nMOS Vt (V)	0.55
Array nMOS Ids/W (uA/um)	400
Array nMOS Leakage (pA/um)	1
Array pMOS Vt (V)	-0.75
Array pMOS Ids/W (uA/um)	-130
Array pMOS Leakage (pA/um)	1

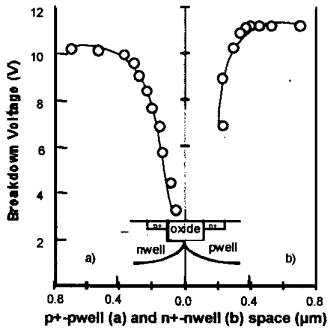

Fig. 3: Breakdown Voltage as a function of interwell spacing, demonstrating solid isolation for a 0.42um p+-n+ spacing

- **Shallow trench isolation**
- **Core and I/O device well formation**
- **70Å I/O oxide grow**
- **High Vt device well formation**
- **DGO patterning *-DGO mask 1***
- **30Å oxide grow**
- **Gate patterning**
- **Core/high-Vt N/PFET LDD**
- **DGO NFET MDD *-DGO mask 2***
- **N/P FET S/D**
- **CobaltSalicide**

Fig. 4: Front end process flow.

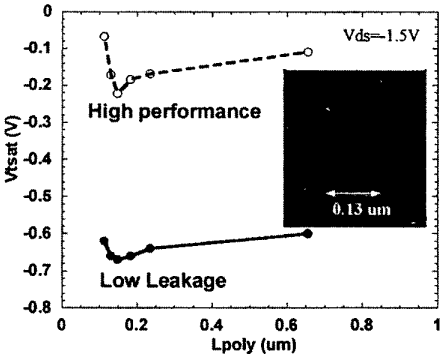

Fig. 5: Vt roll-off for BCPFETs with optimized channel. The 'low leakage' device is used as the load transistor in a 6T SRAM bitcel

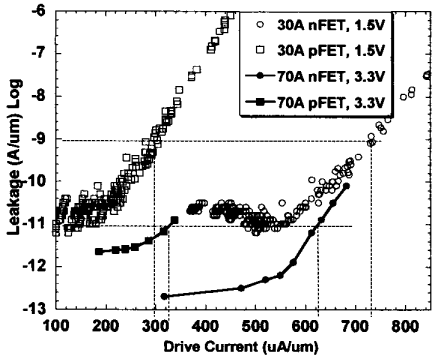

Fig. 6: Ion-Ioff curves for 30 and 70Å n/pFETs.

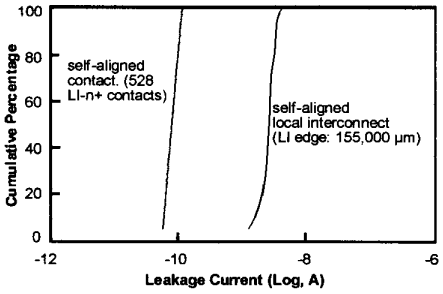

Fig. 7 Leakage current distribution of LI-poly on self-aligned contact and self-aligned LI test structures at 1.5V.

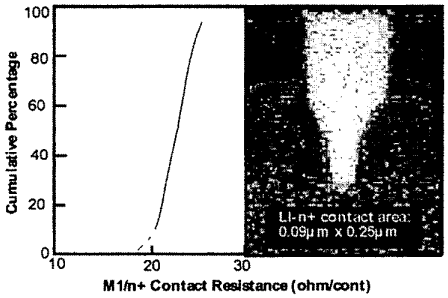

Fig. 8 Contact resistance of a self-aligned contact test structure. The inset shows a SEM cross section of a self-aligned contact.

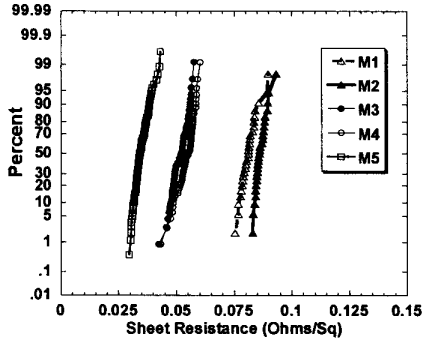

Fig. 9 In-laid Cu interconnect sheet resistances for M1-M5.

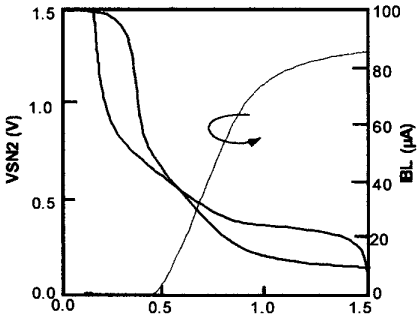

Fig. 10 Butterfly curve of a 2.74μm^2 6T SRAM cell with a cell current of 85 μA and SNM of 220 mV at 1.5 V.

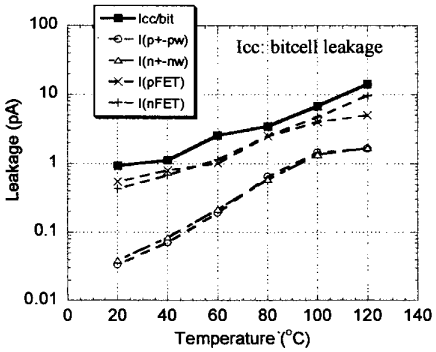

Fig. 11: Bitcell leakage and leakage components of the 2.74 um^2 SRAM bitcell with BCPFET as load and triple well isolation.