Submicron BiCMOS Technologies for Super Computer and High Speed System Implementation

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ABSTRACT
This paper describes submicron process technologies that allow a full implementation of CPU, first level Cache, second level Cache, and the main memory in a BiCMOS approach. CPU Standard Cells up to 100K ECL gate density with embedded CMOS and BiCMOS SRAM, X9 Cache memories, and 1 Meg ECL I/O SRAMs with less than 7ns access time are achieved.

INTRODUCTION
State-of-the-art BiCMOS technologies are vital tools of today's manufacturing and as such they are being extensively used to realize high performance semiconductor products while maintaining high density at moderate power consumption. Due to extra processing steps, cost per wafer for BiCMOS processes is higher than pure CMOS or Bipolar technologies. However, due to performance and density improvement BiCMOS processes enjoy lower cost per gate than ECL at a lower power level, comparable to CMOS products. For memory products BICMOS processes offer higher speed performance along with TTL and ECL I/O options. Using BiCMOS processes tailored for ASIC applications, on the other hand, memory arrays can be incorporated into existing or new designs adding to product versatility and leading to increased performance for systems employing such products.
In this paper two major BiCMOS technology families are discussed and compared in terms of processing and device performance. In addition areas of application for each one of these processes as related to the total system solution will be explored.

ASIC & MEMORY BICMOS FAMILIES
Currently two major high performance BiCMOS technology families exist in National Semiconductors. A technology road map for these process families is shown in TABLE-I. Advanced BiCMOS process family, known as ABiC, is the family of BiCMOS technologies developed for high performance ASIC applications with emphasis on embedded CMOS, BiCMOS or ECL memory as well as BiCMOS and ECL gate array and standard cells. In development of ABiC process, National Semiconductor's state-of-the-art ASPECT process [1,2], has been successfully combined with high performance CMOS process [3,4,5]. The second technology family, known as BiCMOS, is mainly developed for SRAM applications where dense 4T MOS memory cells combined with high speed bipolar logic leads to very high levels of device integration. Final bipolar and CMOS device cross sections for current generation of the ABiC family, ABiC IV, are shown in Fig.1. In Fig.2 process cross section for the 0.8 µm BiCMOS IV technology [6,7] is shown. Despite differences in architecture a high degree of similarity and synergy exists between these processes. Device isolation in both processes is accomplished using an advanced, low encroachment fully recessed oxide isolation process optimized for small bird's beak and planarity as well as defect density. The N+ and P+ twin buried layers form retrograde well profiles for CMOS transistors and result in soft error and latch up immunity. The gate oxide is 150 A thick and in the ABiC IV process is protected by a thin layer of polysilicon during subsequent mask/etch process. The major difference between technologies is in the use of the polysilicon layers.As shown in Fig.1, in the ABiC IV a single layer of polysilicon is used for simultaneous formation of gate, emitter, source/drain and base contacts as well as several high precision poly resistors. The same layer of polysilicon is silicided and used for local interconnection, increasing design flexibility and packing density.
The BiCMOS IV process on the other hand is a double poly technology where the first poly layer forms the gate of the CMOS devices. The second poly layer forms emitter of bipolar transistors as well as high value load resistors for high density 4T cell memory implementation. The area of memory cell in BiCMOS IV is about 37 µm2. The second layer of poly is also selectively silicided, facilitating the formation of low-resistance local interconnects leading to smaller memory foot print and pitch. In contrast, 6T memory cells are more appropriate in ABiC IV where a larger memory cell area of about 100 µm2 can be tolerated. Other key features for these technologies are summarized in TABLE-II.

ELECTRICAL PERFORMANCE
Key device electrical parameters are summarized in TABLE-III. Both technologies enjoy respectable Idsat of 0.4 mA/µm for NMOS and 0.2 mA/µm for PMOS devices and for nominal effective channel length of 0.6 µm. Unity gain frequency, Ft, is about 15 GHz for bipolar transistors. ABiC IV devices , however, have lower extrinsic base resistance as well as S/D resistance due to self aligned silicide. Smaller bipolar foot print in ABiC IV leads to reduced device capacitance as shown in TABLE-III. Gate delay information for ABiC IV and BiCMOS IV are summarized in TABLE-IV. From TABLE-IV both technologies offer similar high performance for CMOS and BiCMOS gates. Delay x power products for several high performance technologies including ABiC IV and BiCMOS IV is given in Fig.3 .ECL performance in ABiC IV technology is superior due to highly optimized bipolar architecture and with gate delay of about 200 psec at 50 µA of current, high levels of integration can be achieved.ABiC IV also offers optimal interconnection performance of less than 1 pS/mil (40 pS/mm) for 4 layers of interconnection.

PRODUCT CAPABILITIES

The BiCMOS process family is primarily designed with high speed and dense SRAM applications in mind. Several high performance memory products such as 256K SRAM [8], 3.5 ns 2Kx9 self timed SRAM [9], 6.8 ns 1MB SRAM with ECL and TTL I/O [10] have been designed in BiCMOS III and BiCMOS IV technologies. The ABiC process, on the other hand, due to smaller and higher performance bipolar devices, is attractive for bipolar intensive applications such as high performance 50 to 120K gates ECL logic array, 100 to 200K gates CMOS/BICMOS logic array and high density ASIC products requiring embedded memories. These two technologies provide a total high-performance system solution. For example Fig.4 illustrates three high speed systems of CPU Standard Cells up to 100K ECL gate density with embedded CMOS and BiCMOS SRAM, X9 Cache memories, and 1 Meg ECL I/O SRAMs with less than 7ns access time .

CONCLUSION

State-of-the-art BiCMOS technologies have been developed leading to total system solutions for high performance applications.

REFERENCES

[1]. A. Iranmanesh *et al*, BCTM Technical Digest, pp 30-32, BCTM, 1989.

[2]. M. Vora *et al*, IEDM Technical Digest, pp 690-694, IEDM, 1984.

[3]. V. Ilderem *et al*, CICC 1990 Proceeding, pp 18.6.1-18.6.4

[4]. A. Iranmanesh *et al*, VLSI 1990.

[5]. A. Iranmanesh *et al*, BCTM 1990.

[6]. W. Burger *et al*, IEDM Technical digest, pp 421, 424 ,IEDM, 1989.

[7]. W. Burger *et al*, BCTM 1990.

[8]. B. Bastani *et al*, Proc. Symp. VLSI Tech. pp 41 -42, VLSI 1987.

[9]. D. Wendell *et al*, VLSI 1990.

[10]. B. Kertis *et al*, VLSI 1990.

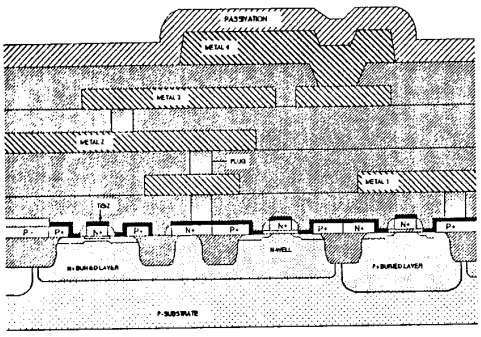

Fig.1 Process Cross section for ABiC IV technology.

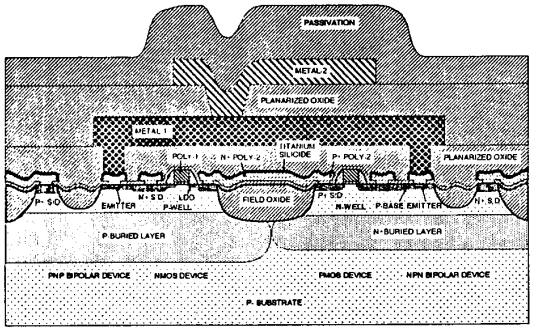

Fig.2 Process Cross section for BiCMOS IV technology.

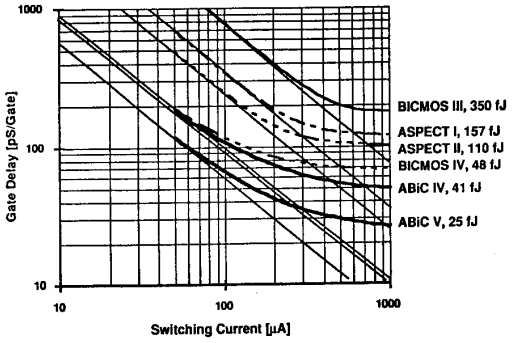

Fig.3 ECL gate Speed x Power product plots for several high performance technologies including ABiC IV and BiCMOS IV.

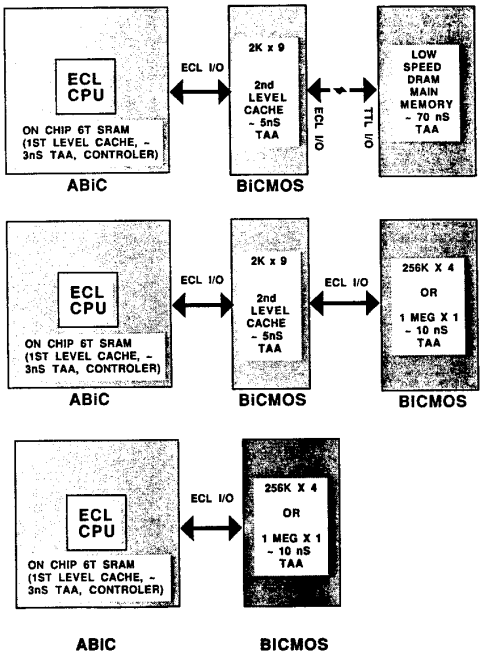

Fig.4 Several high performance system realizations using advanced BiCMOS technologies.

TABLE-I Technology road map for memory and ASIC BiCMOS families.

GENERATION	L [μm]	ASIC BICMOS	LEADING PRODUCT	DATE OF INTRODUCTION
IV	0.8	ABiC IV	100 K ECL/BiCMOS Std Cell+ 156K CMOS SRAM	1990
V	0.5	ABiC V	200 K ECL/BiCMOS Std Cell+ 1Mb CMOS SRAM	1992

GENERATION	L [μm]	MEMORY BICMOS	LEADING PRODUCT	DATE OF INTRODUCTION
III	1.0	BiCMOS III	256 K SRAM	1988
IV	0.8	BiCMOS IV	1 Mb SRAM	1990
V	0.5	BiCMOS V	4 Mb SRAM	1992

TABLE-II Key technology features. Areas of major difference are shown by *.

ABiC IV	BiCMOS IV
*Single Poly	*Double Poly
*6T memory cell	*4T memory cell
*(Area ~ 100 μm2)	*(Area ~ 37 μm2)
Twin Buried Layers	Twin Buried Layers
Retrograde Well	Retrograde Well
PLDD, NLDD	PLDD, NLDD
150 A Gate Oxide	150 A Gate Oxide
Local Interconnect	Local Interconnect
Tungsten Plugs	Tungsten Plugs
*4 Layer Metallization	*2 Layer Metallization
*2.5μm Metal 1,2,3 Pitch	*1.8μm Metal 1 Pitch
High Performance PNP	High performance PNP
*Silicide 1st poly, S/D & Base	
*Integrated Well Tap	
*Several High Precision Resistors	

TABLE-III Key electrical parameters.

PARAMETER	ABiC IV	BiCMOS IV
NPN:		
Emitter Area	0.8 x 1.6 μm2	0.8 x 1.5 μm2
Beta	90	150
BVebo	6 V	3.6 V
BVcbo	15 V	14 V
BVceo	8 V	6 V
Cjeb	3.3 fF	5.6 fF
Cjcb	2.9 fF	5.2 fF
Cjcs	10.2 fF	16.2 fF
Ft	15 GHz	15 GHz
CMOS:		
Leff	0.6 μm	0.6 μm
Vtn	0.75 V	0.75 V
Vtp	-0.95 V	-0.95 V
Idsat, NMOS	0.4 mA/μm	0.4 mA/μm
Idsat, PMOS	0.2 mA/μm	0.2 mA/μm

TABLE-IV Summary of ring oscillator gate delay values for BiCMOS IV and ABiC IV processes.

GATE TYPE	DELAY [pS], CL=0		DELAY [pS], CL=1.0 pF	
	ABiC IV	BiCMOS IV	ABiC IV	BiCMOS IV
CMOS	89	86	480	491
BICMOS	125	122	320	341
ECL (1mA)	48	65	138	157
ECL (200 μA)	72	85	232	250