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ADVANCED ONE MICRON BiCMOS TECHNOLOGY FOR HIGH SPEED 256K SRAMS

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INTRODUCTION
The MOS technology produces the most straight forward and the highest density memory array for SRAM technology. The ECL process, however, dominates the high performance arena at the cost of power dissipation and density. A well orchestrated combination of these two technologies with proper design methodology results in high speed memories and logic products with specific performance targets that neither technology could deliver alone (1)-(3). It is for such applications that BiCMOS technology provides the optimum solution. In this paper an advanced one micron BiCMOS technology optimized for a high speed 256K SRAM is described. Transistor optimizations for MOSFET and bipolar devices are presented herein. Ring oscillators, memory array and functional subcircuits have been fabricated to verify the performance of the technology.

TECHNOLOGY
The one micron BiCMOS process is an optimized 16 mask, double poly Si, double metal sequence. Figure 1 illustrates a cross section of the device. Tables I and II outline the processing sequence and key technology features respectively. Self-aligned twin buried layer initially defines the N-channel, P-channel, and bipolar device areas. The P- buried layer results in improved isolation spacing, N-MOSFET performance, and soft error immunity. The N+ buried layer is formed by As implantation. The lower activation temperature required for As compared to more conventional Sb doping reduces collector sidewall capacitance and allows higher performance bipolar transistors to be achieved.
A 1.5 micron intrinsic reduced pressure epi is grown on top of the twin buried layers. Self-aligned twin N- and P- wells are formed in this thin epi layer. Active regions are formed by an optimized LOCOS process resulting in less than 0.3μm bird's beaks.
LDD MOSFET devices are fabricated with 200 A gate oxide. A processing sequence of L_{DD} implant, HTO spacer oxide formation, N+ S/D and anneal, bipolar base implant, and P+ S/D implant complete the MOSFET and partial bipolar transsitor formations.
The emitter window for the bipolar transistor is opened in the HTO interpoly dielectric prior to poly 2 deposition. The butting contact in the memory array is also formed in this process step. Various bipolar optimization approaches have been exercised at the emitter formation in order to reduce poly emitter interface resistance, base resistance and junction capacitances. LPCVD BPSG glass technology is utilized to minimize thermal process history in the formation of device interconnects. Low temperature reflow characteristics of an optimized BPSG film provide for a high density interconnect technology and near planar metal-1 topography. A sandwiched Al-Si-Cu barrier metallurgy produces a reliable and hillock-free interconnect system. The same metallurgy is used for the second layer metal. Fig. 2 shows a SEM cross section of the 256K memory array where compacted bird's beak, poly 1, poly 2, and the metal-2 layer on a planarized surface are featured.

DEVICE CHARACTERISTICS

a) MOSFET
The impurity profiles for N- and P- channel MOSFET are illustrated in Fig. 3. The P- buried layer shunts the MOSFET parasitic source-drain lateral bipolar transistor. As a result, the impact-ionization induced breakdown for even subhalf micron N-MOSFET, is highly suppressed. The punchthrough voltage versus the effective channel length for the illustrated profiles are given in Fig. 4. A minimum effective channel length of .6μm for N- channel and .7μm for P-channel are representative of this process.

b) BIPOLAR TRANSISTOR
Two approaches were investigated for the bipolar transistor involving As and P dopants to form the poly emitter. The phosphorous disadvantage is a deeper emitter junction (0.22μm) compared to arsenic (0.12μm). The P advantage, however, is a lower emitter interfacial series resistance of 90 Ω-μ^2 as opposed to 250 Ω-μ^2. Typical poly emitter bipolar characteristics are shown in Fig. 5. Flat h_{fe} characteristics over 4 decades of collector current and excellent ICEO behavior are evidenced.

c) RING OSCILLATOR
CMOS, ECL and BiCMOS ring oscillators under various loading conditions were used to benchmark the technology. Table III shows gate delays under unloaded and loaded conditions.

RELIABILITY
Electromigration: MTTF in excess of 200 years were achieved for the barrier metallurgy at M-1 design rules.
Soft Error: A 3X reduction in charge collection was achieved at N+ nodes as a result of P+ buried layer.

256K SRAM
A symmetric .96μ^2 NMOS memory cell with a polysilicon load is used for the static RAM array. Extensive use of ECL circuitry provides the basis for a high speed design. The 256K SRAM is organized in a 16K modular format. Fig. 6 shows a die layout photograph of a 16K SRAM.

SUMMARY
One micron BiCMOS technology for high speed 256K SRAM is developed. Advanced lithography and processing techniques support high density CMOS design with ECL performance. This technology is also extended to logic applications.

TABLE I PROCESS SEQUENCE OUTLINE

o twin buried layer	o interpoly contact/emitter
o twin well	o poly 2
o LOCOS isolation	o emitter/resistor implant
o poly 1	o contact
o LDD	o metal-1
o n+ S/D implant	o via
o base	o metal-2
o p+ S/D implant	o topside passivation

TABLE II KEY TECHNOLOGY FEATURES

o 16 masks	o 0.8µm resol. 5X stepper
o optimized LOCOS	o 0.9µm isolation spacing
o 200 A gate oxide	o L_{DRAWN} = 1.1µm
o double poly Si	o 2.2µm poly pitch
o double metal	o 2.5µm metal-1 pitch
o 1.1X1.1µm contacts	o 1.1X1.1µm vias

TABLE III GATE DELAYS

	Unloaded	0.5 pf
CMOS	165ps	540ps
ECL	250ps	320ps
BiCMOS	280ps	380ps

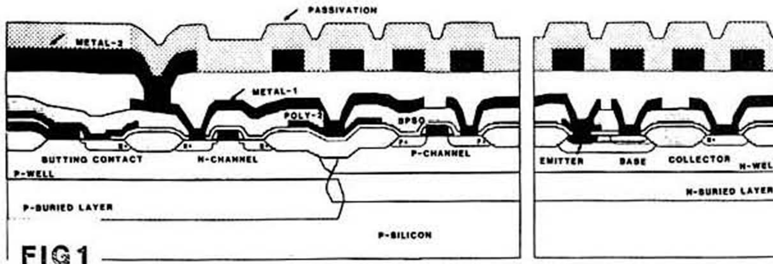

FIG1

REFERENCES

1) N. Nishio, et al; ICCD 1984
2) A. Watanabe, et al; IEDM 1985
3) A.R. Alvarez, et al;IEDM 1984

FIGURES

1) Schematic device cross-section
2) Memory array SEM cross-section
3) N- and P-channel impurity profiles
4) MOSFET punchthrough vs L_{EFF}
5) Poly-emitter bipolar characteristics
6) Layout photograph of 16K die

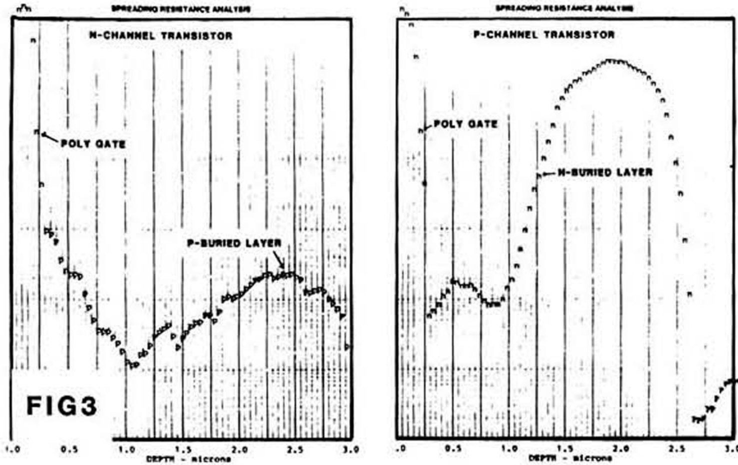

FIG3

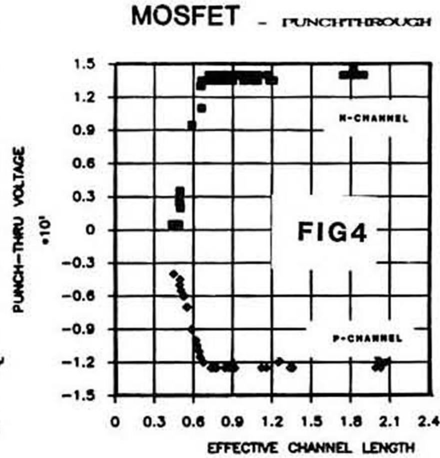

FIG4

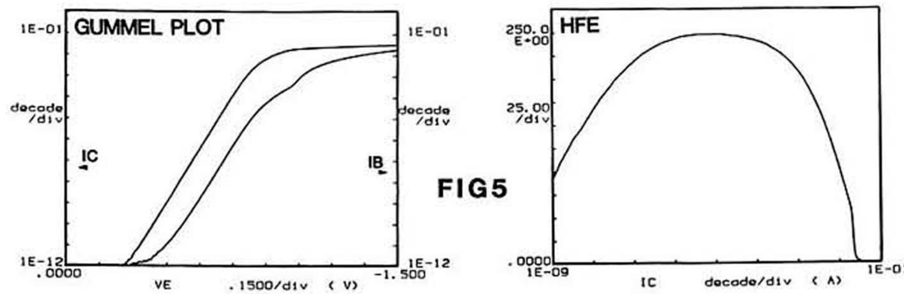

FIG5

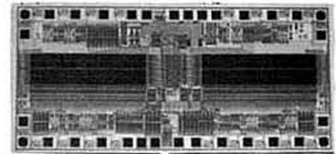

FIG6

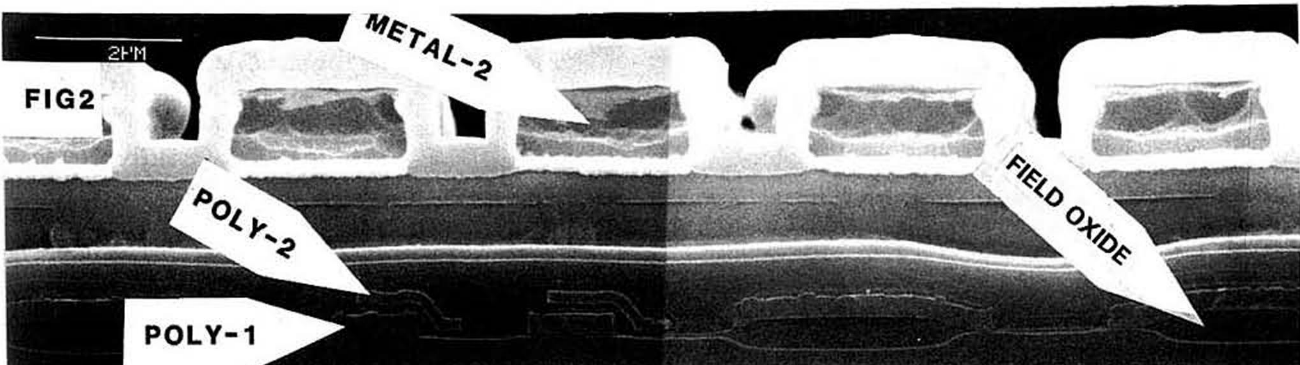

FIG2