Craig Lage

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SUMMARY

After a successful career in microelectronics, I am currently working as a Postdoctoral Researcher in astrophysics. I have a broad background in physics, astronomy, and electronics.

EDUCATION

Doctor of Philosophy, Physics with astrophysics focus
New York University, New York, NY — September, 2014
THESIS - A detailed simulation of the Bullet Cluster collision.
GPA 3.78/4.0

Master of Science, Electrical Engineering
University of Wisconsin, Madison, Wi — June, 1979
THESIS - Design and construction of a concentric array of silicon photodiodes.
GPA 3.85/4.0

Master of Science, Nuclear Engineering
University of Wisconsin, Madison, Wi — June, 1978
GPA 3.53/4.0

Bachelor of Science, Physics
California Institute of Technology (Caltech), Pasadena, Ca — April, 1976
GPA 3.5/4.0

TEACHING EXPERIENCE

Adjunct Professor - NYU — Spring 2014

Taught the undergraduate Observational Astronomy course at NYU. This included lectures, indoor lab sessions, and observational lab sessions. Course website available at `http://lage.physics.ucdavis.edu/obs_astro.html`.

Graduate Teaching Assistant - NYU — Fall 2013

TA in the graduate level course in Computational Physics.

Adjunct Professor - Hunter College - New York, NY — Spring 2013

Had full responsibility for organizing and teaching Physics 222 - Undergraduate Electronics Laboratory. Student Evaluations were quite high, with an average score of 6.3/7.0.

After School STEM Mentor — Spring 2013

Volunteer position teaching Space Science at Lower Manhattan Community Middle School.

Undergaduate Teaching Assistant - NYU Fall 2009 - Spring 2011

Had Teaching Assistant responsibility for four undergraduate courses:

- Quarks to Cosmos, How Things Work, General Physics Laboratory, Observational Astronomy

PROFESSIONAL EXPERIENCE

University of California - Davis: Department of Physics 2014 - Present

My current postdoctoral work involves the CCD detectors for the Large Synoptic Survey Telescope (LSST). This innovative new telescope, currently under construction at Cerro Pachon in Chile, will survey the entire southern sky to unprecedented depth. A key component of the telescope is the 3.2 Gigapixel digital camera, one of the largest cameras ever built. My work involves characterizing and modeling the astrometric and photometric distortions of the CCD detectors used in the camera, in order to ensure that the data produced by the LSST survey will be of the highest possible quality. I am also doing hands-on assembly of some of the camera components.

Freescale Semiconductor (formerly Motorola) 1990 - 2008

Held a variety of technical management positions of increasing responsibility involving development and transfer to manufacturing of advanced CMOS semiconductor technologies, primarily for computing, networking and cellular phone applications. At its largest, the group I managed consisted of over 100 technical professionals

Fairchild Semiconductor / National Semiconductor 1985 - 1990

Was responsible for the process integration and transfer to manufacturing of BiCMOS SRAM technologies. At the time, our organization developed some of the highest performance memories in the world.

Hewlett-Packard 1979 - 1985

Held positions in technology development and technical management focused on development of advanced CMOS technologies and products.

COMPUTER SKILLS

Proficient in Unix, Python, Mathematica, C/C++. Some experience with Fortran. Also capable in Microsoft Windows and Microsoft Office environments.

PUBLICATIONS

Full text of the publications listed below are available at my web site: `http://lage.physics.ucdavis.edu`.

Astrophysics

- Lage, C., Bradshaw, A.K., Tyson, J.A., "Poisson CCD: A dedicated simulator for modeling CCDs", Available on the arXiv at `http://arxiv.org/abs/1911.09038v1`.

- Lage, C., "Physical and electrical analysis of LSST sensors", Available on the arXiv at http://arxiv.org/abs/1911.09577v1.
- Lage, C., "Linearity and correction of the BF effect in LSST sensors", Available on the arXiv at http://arxiv.org/abs/1911.09567v1.
- Bradshaw, A.K., Lage, C., Tyson, J.A., "Characterization of LSST CCDs Using Realistic Images, Before First Light". Available on the arXiv at http://arxiv.org/abs/1808.00534v1.
- Lage, C., Bradshaw, A., Tyson, J.A., "Measurements and Simulations of the Brighter-Fatter Effect in CCD Sensors", JInst, V12, PC03091, 2017. Available on the arXiv at http://arxiv.org/abs/1703.05823.
- Villasenor, J., et.al., "Reach-through Effect in Deep Depletion TESS CCDs", JInst, V12, P04025, 2017.
- Rasmussen, A., et.al., "High fidelity point-spread function retrieval in the presence of electrostatic, hysteretic pixel response", Proceedings of the SPIE, Vol 9915, 2016. Available on the arXiv at http://arxiv.org/abs/1608.019642v2.
- Shimwell et.al., "Another shock for the Bullet cluster, and the source of seed electrons for radio relics.", MNRAS, N449, May, 2015. Available on the arXiv at http://arxiv.org/abs/1502.01064.
- Bradshaw et.al., "Mapping charge transport effects in thick CCDs with a dithered array of 40,000 stars", Journal of Instrumentation, V10, Apr, 2015. Available on the arXiv at http://arxiv.org/abs/1507.02683.
- C. Lage, G.R. Farrar, "The Bullet Cluster is not a Cosmological Anomaly", JCAP, V2, P38, 2015. Available on the arXiv at http://arxiv.org/abs/1406.6703.
- Shimwell et.al., "Deep radio observations of the radio halo of the bullet cluster 1E 0657-55.8"¡/a¿. MNRAS, V440, Jun, 2014. Available on the arXiv at http://arxiv.org/abs/1403.2393.
- C. Lage, G. Farrar, "Constrained Simulation of the Bullet Cluster", Astrophysical Journal, 787(2):144, 2014. Available on the arXiv at http://arxiv.org/abs/1312.0959v1.
- C. Lage, G. Farrar, "Multi-Wavelength Simulation of the Bullet Cluster", presented at the meeting of the American Astronomical Society, Austin, Tx, 2012.
- C.S. Lage and W. Whaling, "Transition Probabilities in Pr(II) and the Solar Praseodymium Abundance", Journal of Quantitative Spectroscopy and Radiative Transfer, Vol 16, pp 537-542, 1976.

Partial list of microelectronics publications

- H.S. Yang, et.al., "Scaling of 32nm Low Power SRAM with High-K Metal Gate", IEEE IEDM Proceedings, Dec., 2008.
- X. Chen, et.al., "A Cost Effective 32nm High-K/ Metal Gate CMOS Technology for Low Power Applications with Single-Metal/Gate-First Process", Proceedings of the Symposium on VLSI Technology, 2008.
- C. Lage, J.D. Hayden, C. Subramanian, "Advanced SRAM Technology The Race Between 4T and 6T Cells", IEEE IEDM Proceedings, Dec., 1996.
- S. Venkatesan, J.W. Lutze, C. Lage, W.J. Taylor, "Device Drive Current Degradation Observed with Retrograde Channel Profiles", IEEE IEDM Proceedings, Dec., 1995.
- C. Lage, D.Burnett, T.McNelly, K.Baker, A.Bormann, D.Dreier, V.Soorholtz, "Soft Error Rate and Stored Charge Requirements in Advanced High-Density SRAMs", IEEE IEDM Proceedings, Dec., 1993.
- S.Poon, C. Lage, "A Trench Isolation Process for BiCMOS circuits", IEEE BCTM Proceedings, Oct., 1993.

- D. Burnett, C. Lage, A. Bormann, "Soft-Error-Rate Improvement in Advanced BiCMOS SRAM's", IEEE IRPS Proceedings, Apr., 1993.
- C. Lage, "BiCMOS Process Technology for High-Speed Four Megabit SRAMs", GOMAC Digest of Technical Papers, Nov., 1992.
- Yeong-Seuk Kim, David Burnett, and Craig S. Lage, "New Method for Determining the Reverse Transit Time in Bipolar Transistors", IEEE Transactions on Electron Devices, Oct., 1992.
- Craig Lage, "BiCMOS Memories: Increasing Speed While Minimizing Process Complexity", Solid State Technology, Aug., 1992.
- J.D. Burnett, C. Lage, J. D. Hayden, "Bipolar Reliability Optimization Through Surface Compensation of the Base Profile", IEEE IRPS Proceedings, Apr., 1992.
- W.R. Burger, C. Lage, B. Landau, M. DeLong, J. Small, "An Advanced 0.8 m Complementary BiCMOS Technology for Ultra-High Speed Circuit Performance", IEEE BCTM Proceedings, Oct., 1990.
- S.P. Joshi, R. Lahri, C. Lage, "Poly Emitter Bipolar Hot Carrier Effects in an Advanced BiCMOS Technology", IEEE IEDM Proceedings, pp 182-185, Dec., 1987.
- B. Bastani, C. Lage, L. Wong, J. Small, R. Lahri, L. Bouknight, T. Bowman, J. Maniliou, P. Tuntasood, "Advanced One Micron BiCMOS Technology for High Speed 256K SRAMS", Proceedings of the Symposium on VLSI Technology, pp 41-42, 1987.
- K.Y. Chiu, J.L. Moll, K.M. Cham, J. Lin, C. Lage, S. Angelos, R.L. Tillman, "The Sloped-Wall Swami - A Defect-Free Zero Bird's-Beak Local Oxidation Process for Scaled VLSI Technology", IEEE Transactions on Electron Devices , pp 1506-1511, 1983.

PATENTS

- Craig S. Lage, James E. Small, and Bamdad Bastani, "Process for Fabricating High Performance BiCMOS Circuits", US. Patent 5,079,177, Filed Sept. 19, 1989, Issued Jan. 7, 1992.
- Craig S. Lage and Richard D. Sivan, "Semiconductor Memory Cell Having a Trench Structure", US. Patent 5,285,093, Filed Oct. 5, 1992, Issued Feb. 8, 1994.
- Craig S. Lage, "Ferromagnetic Memory Device", US. Patent 5,329,486, Filed Jul. 23, 1993, Issued Jul. 12, 1994.
- Craig S. Lage , "Process for Fabricating a Self-Aligned Interconnect Structure in a Semiconductor Device", US. Patent 5,360,757, Filed Mar. 3, 1993, Issued Nov. 1, 1994.
- Craig S. Lage, Frank K. Baker, James D. Hayden, Kent J. Cooper, "Process for Forming an Integrated Circuit", US. Patent 5,377,139, Filed Dec 11, 1992, Issued Dec 27, 1994.
- Craig S. Lage , "A Method of Forming a Ferromagnetic Memory Device", US. Patent 5,389,566, Filed Mar. 28, 1994, Issued Feb. 14, 1995.
- Craig S. Lage , "Process for Forming a Static Random Access Memory Cell", US. Patent 5,422,296, Filed Apr. 20, 1994, Issued June 6, 1995.
- Craig S. Lage, Frank K. Baker, James D. Hayden, Kent J. Cooper, "Static Random Access Memory Cell and an Integrated Circuit Having a Static Random Access Memory Cell", US. Patent 5,485,420, Filed July 21, 1994, Issued Jan 16, 1996.
- Craig S. Lage , "Static Random Access Memory Cell", US. Patent 5,489,790, Filed Jan. 30, 1995, Issued Feb. 6, 1996.
- Craig S. Lage , "Semiconductor Device Including a Memory Cell and Peripheral Portion and Method for Forming Same", US. Patent 6,100,568, Filed Nov. 6, 1997, Issued Aug. 8, 2000.

- Craig S. Lage, Mousumi Bhat, Yeong-Jyh Tom Lii, Andrew G. Nagy, Larry E. Frisa, Stanley M. Filipiak, David L. OMeara, T.P. Ong, Michael P. Woo, Terry G. Sparks, Carol M. Gelatos, "Process for Forming a Semiconductor Device Having an Interconnect or Conductive Film Electrically Insulated from a Conductive Member or Region", US. Patent 6,184,073, Filed Dec. 23, 1997, Issued Feb. 6, 2001.
- Craig S. Lage , Michael P. Woo, Hong Tian, Xiaodong Wang, "Method of Forming a Semiconductor Device with Isolation and Well Regions", US. Patent 6,440,805, Filed Feb. 24, 2000, Issued Aug. 27, 2002.
- Craig S. Lage , "Magnetic Random Access Memory having a Vertical Write Line", US. Patent 6,621,730, Filed Aug. 27, 2002, Issued Sep. 16, 2003.
- Craig S. Lage , et.al., "Semiconductor device, memory cell, and process for forming them", US. Patent 6,686,633, Filed Aug. 31, 2000, Issued Feb. 3, 2004.
- Bami Bastani, Craig Lage, Larry Wong, "Process for fabricating bipolar and CMOS transistors on a common substrate", European Patent EP0369336A2, Filed Nov. 10, 1989, Issued May 23, 1990.
- Craig S. Lage , James E. Small, Bamdad Bastani "Process for fabricating high-performance BiMOS circuits", European Patent EP0418670B1, Filed Sep. 7, 1990, Issued Mar. 19, 1997.

PUBLICLY RELEASED SOFTWARE

- Craig Lage, "A simple grid-based Poisson's equation solver to simulate pixel distortion effects in thick fully-depleted CCD's for the LSST digital camera.", `https://github.com/craiglagegit/Poisson_CCD`
- Craig Lage, "Code for controlling the f/1.2 LSST Optical Simulator at UC Davis", `https://github.com/craiglagegit/LSST_GUI`
- Craig Lage, "Code for building masks containing a combination of simulated stars and galaxies", `https://github.com/craiglagegit/MaskCode`

HONORS

- Received the James Arthur Graduate Fellowship at NYU in 2013.
- Served as General Chairman of the 2002 Symposium on VLSI Technology, an international technology conference held annually in the United States and Japan
- Selected as a Dan Noble Fellow, Motorola′s highest technical honor, in 2001

PERSONAL

- US Citizen
- Languages - Native English speaker, fluent in French, capable in German. Learning Spanish.
- Hobbies - Cycling, Woodworking.